

Pre-Thesis :

Detector Front-End and Burst-Mode Clock and Data Recovery ASIC Design for HEP Instrumentation

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Abstract

Experimental physics is about developing instrumentation and interpreting the data coming out of that instrumentation, usually in very large scale. From the physics phenomena down to interpretation of the results, there is a strongly connected chain of links including detector development, design of front-end (FE) Application Specific Integrated Circuits (ASICs), read-out systems, communication architectures, data acquisition (DAQ) and monitoring softwares, and implementation of frameworks for off-line analysis.

In this brief, an overview of detector FE electronics and burst-mode capable Clock and Data Recovery (Burst-CDR) chips for transceivers intended for nuclear and High Energy Physics (HEP) experiments will be considered. Work done for CMAD ASIC and GBT transceiver will be presented.

I. INTRODUCTION

Modern particle detectors employ highly integrated and custom designed electronics. High integration is needed because of required detection precision in terms of time and spatial resolutions. The space allowed for the electronics due to required detector granularity is also a severe concern. Even though, almost any kind of building blocks are available commercially, they are not optimized and compiled onto chips dense enough in accordance to High Energy Physics (HEP) requirements. Thus, building an experimental HEP system composed of commercial components exceeds most of the form factor standards in the field. Custom design is needed because of the inexistence of commercially available chips which could be used for specific functionality required by experimental systems. Also the heavily radioactive environment leads to custom layout design, since commercial products are not built for radiation hardness[19]. Using special layout techniques[1][2] to make the circuits radiation tolerant is a decision made at the cost of relatively bigger and, thus, slightly slower layouts.

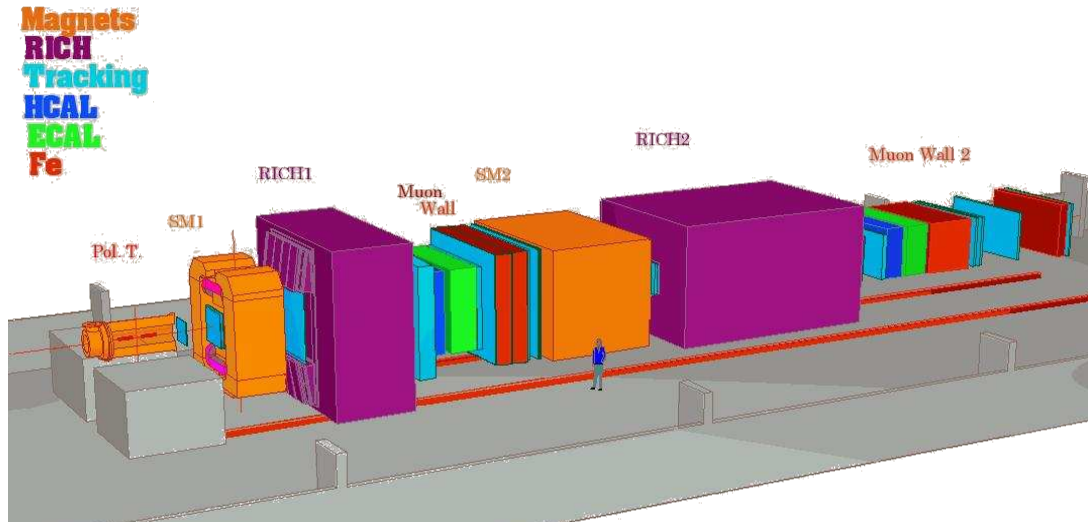


Fig. 1. The COMPASS experiment at CERN-SPS

II. DETECTOR FRONT-END

In nuclear and HEP instrumentations, FEs form the interface between the detector and read-out system. Data are transferred through read-out channels (ROC) and FEs provide the first analog interpretation of the detection. They establish functions like signal amplification and shaping, channel equalization, quantization and zero suppression. After FEs encapsulate raw data in a proper way, read-out takes over and the data flows to the next destination through DAQ system.

Based on the content of what is being detected, FEs may have significantly different requirements which imposes application specific architectural choices. The energy region of interest and statistical requirements defining the speed of the channel have also severe impact on architectural choices.

A common example could be the binary read-out (BRO) architectures which come with the difficulty of producing identical-enough read-out channels. BRO architecture is commonly used in tracking detectors for nuclear and HEP experiments. In this architecture, each single detector component (e.g. one pad of an array of pads located on a planar surface) is expected to produce "yes" or "no" information as result of a detection. The detected analog value is amplified-shaped-compared to a reference value and depending on the comparison result the binary signal is sent to the next stage on the chain. As shown in Fig. 3, the input stage could be a charge sensitive amplifier (CSA) normally formed by an integrator followed by a shaper. As soon as the signal at the output of the front-end exceeds a certain value (i.e. threshold of the comparator, adjusted by a D/A) due to the charge provided by the detector, the comparator triggers a logic pulse. The pulse is, then, further processed by the next stage, e.g. a counter CN.

In the next section, a BRO FE ASIC using such an architecture for RICH-1 detector system for COMPASS experiment at CERN-SPS is presented.

A. "CMAD", a Full Custom ASIC for the Upgrade of COMPASS RICH-1

An 8 channel, full-custom ASIC prototype, named "CMAD", has the task of amplifying the signals coming from fast multi-anode photomultipliers and comparing them against a threshold adjustable on-chip on a channel by channel basis.

CMAD, developed using a 350nm commercial CMOS technology, occupies an area of $4.7 \times 3.2 \text{ mm}^2$ and consumes 26 mW/Ch power from a 3.3 V single source.

COMPASS [12] is an experiment at the CERN SPS designed to study the structure and spectroscopy of hadrons with diverse types of high intensity beams. One of the key components of the experimental apparatus is a Ring Imaging Cherenkov (RICH) detector, used to perform particle identification (See Fig. 1 and Fig. 2).

In order to improve the reconstruction efficiency of the RICH, an upgrade is under development [13]. The experience gained with the first physics runs has, in fact, shown that a trigger rate of 100 kHz and a single channel rate of 5 MHz should be sustained in order to reach optimal performance. These tight requirements can be achieved by detecting the photons produced in the sensitive volume by photomultiplier tubes equipped with fast read-out electronics. The granularity of the system demands the use of compact multi-anode photomultipliers (MPT). The increased event rate that the system has to cope with has motivated the development of a new FE ASIC. This chip will replace the MAD-4 [14] used in the read-out of the RICH-I by the time of this brief.



Fig. 2. The CERN-SPS

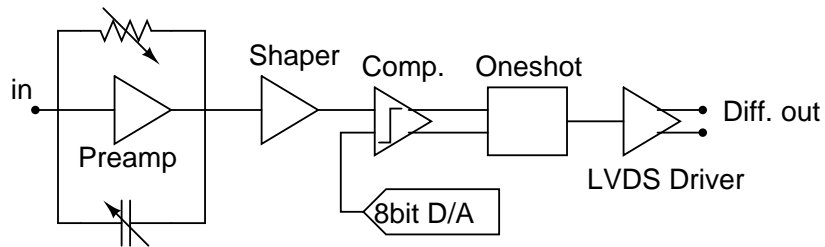


Fig. 3. Binary read-out architecture of a single channel.

B. Architecture

Fig. 3 shows the architecture of a single channel. Each processing channel features a low-noise transimpedance amplifier followed by a shaper with 10 ns peaking time, a baseline restorer, a comparator, a programmable oneshot and an LVDS driver.

The gain of the preamplifier can be adjusted from 0.4 mV/fC to 1.2 mV/fC in steps of 0.08 mV/fC. This allows to compensate at least partially for the channel-to-channel gain variation of the MPTs. Additionally, the threshold of each comparator can be adjusted on a channel by channel basis via a local 8-bit digital to analog converter (D/A). The gain of the front-end and the D/A codes are programmed using a digital control unit and the I2C standard.

The fast shaper shown in Fig. 4 is based on a class AB operational amplifier [15] around which two feedback networks are implemented. A fast path performs high frequency filtering while a slow feedback provides the AC coupling with the previous stage and guarantees baseline stabilization [16].

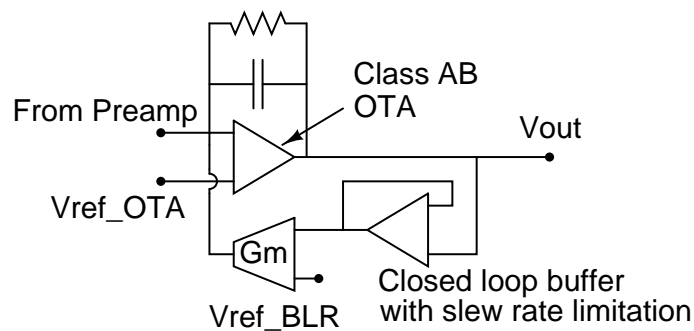


Fig. 4. Architecture of the shaper in the channel.

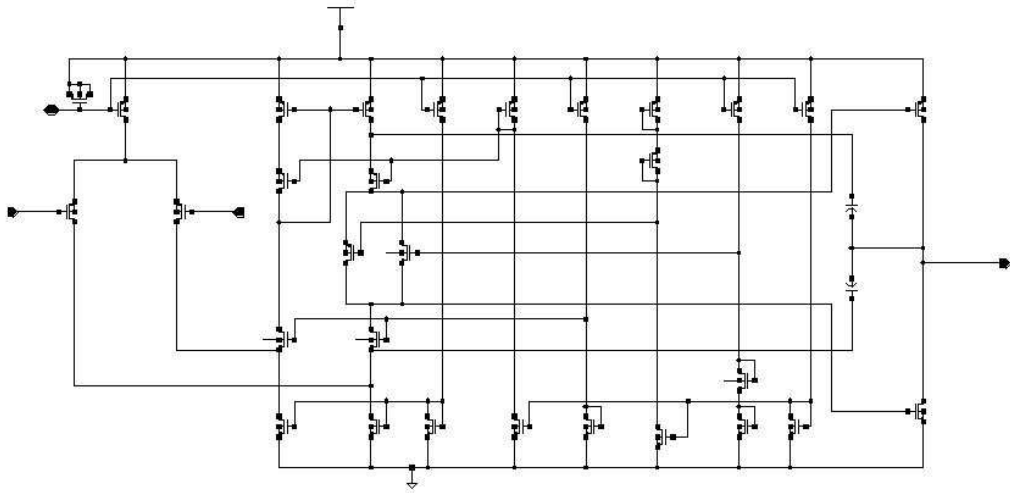


Fig. 5. CMOS AB class OTA.

A fast unity gain buffer with limited slew rate is used in the baseline control loop. Fast output signals at the output of the shaper are clipped before arriving at the transconductor stage. The baseline stabilization circuit is designed to reduce the baseline shift to less than 3 mV for output pulses with a 3 V amplitude and 10 MHz rate.

The peaking time at the output of the shaper is 10 ns . The system has been designed to cope with a rate in excess of 5 MHz/Ch . The output pulses are stretched by a programmable one-shot and sent to an output stage able to drive long twisted pair cables with LVDS compatible levels (Fig. 3).

C. Circuit Design

Fig. 5 shows the implementation of OTA used within the shaper. The class AB CMOS OTA circuit dissipates 3 mW of static power from a 3.3 Volts power supply and drives a 10 pF load with a slew rate of more than $500\text{ V}/\mu\text{s}$.

In the binary architecture given in Fig. 3, a global D/A can not be used since each of the read-out channels needs its own comparator that operates independently from the rest. This brings the necessity of a low power and small area D/A architecture, since it would be used for each read-out channel and thus more than once per chip.

Conceptually, the simplest D/As use a binary-weighted architecture, where n -binary weighted elements (current sources, resistors or capacitors) are combined to provide an analog output ($n = \text{D/A resolution}$). Digital encoding circuits are minimized, but the difference between the MSB and the LSB weights increase with increasing resolution, making accurate element matching difficult.

Among others like Kelvin divider or segmented architectures, the R-2R, or ladder, architecture relaxes component-matching requirements since only two component values are required in a 2:1 ratio. The R-2R architecture can be configured as a voltage- or current-mode D/A, together with different advantages and disadvantages.

A drawback of a current-mode R-2R architecture is the inversion introduced by the opamp which usually exists as an output current-to-voltage converter. Another disadvantage is the complicated stabilization of the opamp due to the fact that the D/A output impedance varies with digital input code. Current mode operation also results in higher glitch, since the switches connect directly to the output.

Advantage of voltage-mode R-2R configuration is that the output voltage has constant impedance, thus simplifying amplifier stabilization. Glitch generated by switch capacitance is also minimized. The drawback of voltage-mode R-2R configuration is that the reference input impedance varies widely, so a low-impedance reference must be used. Also, the switches operate from ground to V_{ref} , restricting the allowed range of the reference.

CMAD implementation employs Low Drop-Out regulators (LDOs) for setting the reference voltage and bias current of the D/A together with other blocks. The technology used ($0.35\text{ }\mu\text{m}$) has relatively a high analog performance compared to recent low feature size technologies, so the amplifier compensation is easily achievable for the whole operation range. Relatively a high accuracy of matching is also feasible with proper layout.

Concerning the above discussion, CMOST-only current-mode R-2R architecture is a suitable solution as it is composed of only transistors that are compact and that consume very low power. An important concern is also the output impedances driving the comparator, namely the outputs of the shaper and the D/A. For proper functioning of the comparator input stage which is

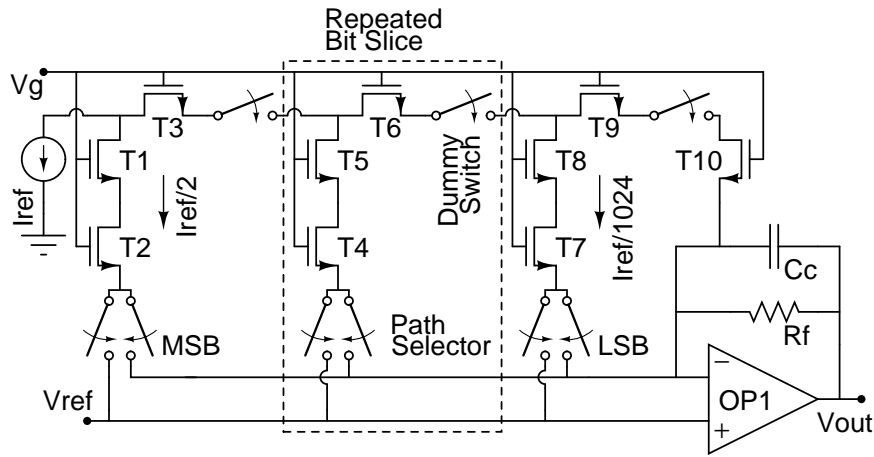


Fig. 6. 10b CMOS-Only R-2R architecture.

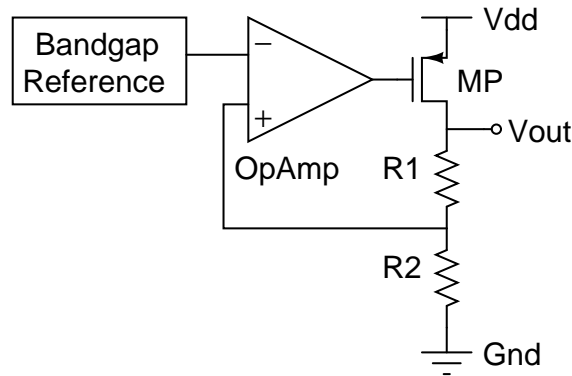


Fig. 7. LDO voltage reference.

basically a differential pair, it is desired to equalize these impedances. The shaper has a low output impedance, thus requiring the same for the D/A.

Fig. 6 shows conceptually the architecture of the small area-low power 10-bit D/A used for setting the threshold of the comparator [17]. In such an architecture, transistors in the ladder do not necessarily emulate identical resistor values but instead, successful operation is based on linear current division principle [18]. The accuracy of the division technique used is based on the characteristic I-V curve matching of the two transistors but not on their linearity [3].

In operation, first two MSBs are set globally together with the base line and the effective resolution required by the channel is 8 bits. Additional pads are also provided for the flexibility of disabling the on-chip LDO reference to be able to apply external sources. The LSB, thus the resolution, of the D/A can be adjusted for different conditions, in this way.

Power consumption of the D/A in Fig. 6 is approximately 1.1 mW including the opamp. A current mirror implementation with the same functionality and power consumption would exhibit a much larger output impedance. CMOS-only R-2R core operates with 50 μ A of current which is negligible compared to the one consumed by the opamp.

On-chip biasing is implemented via reference sources based on LDOs driven by band-gap voltage sources, as seen in Fig. 7. Linear voltage regulators use an active pass element (MP) to reduce the input voltage (Vdd) to the regulated output voltage (V_{OUT}). Linear voltage regulators force a fixed voltage level to appear at the output terminal.

The LDOs implemented for CMAD are optimized for sub-circuit requirements and consume 0.9 mW from 3.3 V single source.

Fig. 8 shows the implementation of the opamp-less band-gap reference driving the LDOs. The reference voltage output is given as $V_{REF} = V_{BE3} + 5V_T \ln(n)$ where V_{BE3} is the B-E potential difference of Q3, V_T is the thermal voltage and n ($=33$) is the area ratio between Q2 and Q1. Band-gap in Fig. 8 consumes 93 μ W from 3.3 V single source.

D. Case Study - Example of Architectural Comparison

Before transistor level implementation, architectural comparisons must be done. Behavioural model is ideally created and checked based on the requirements. This subsection gives an example of how two architectures are compared in an ideal

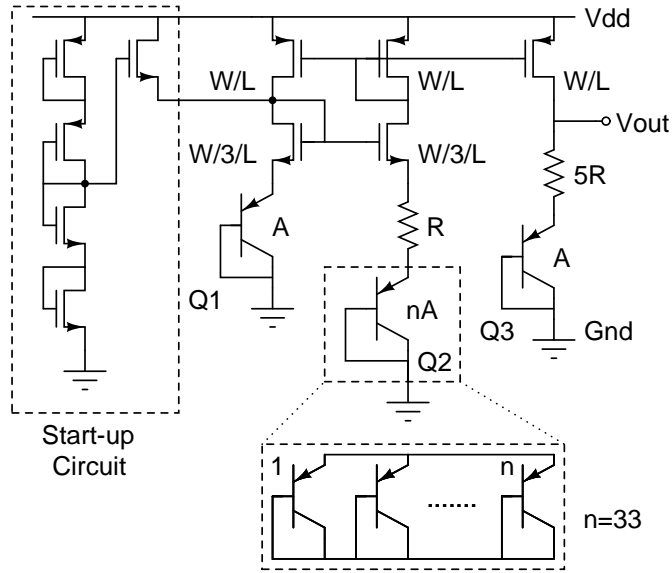


Fig. 8. Implemented opamp-less band-gap reference.

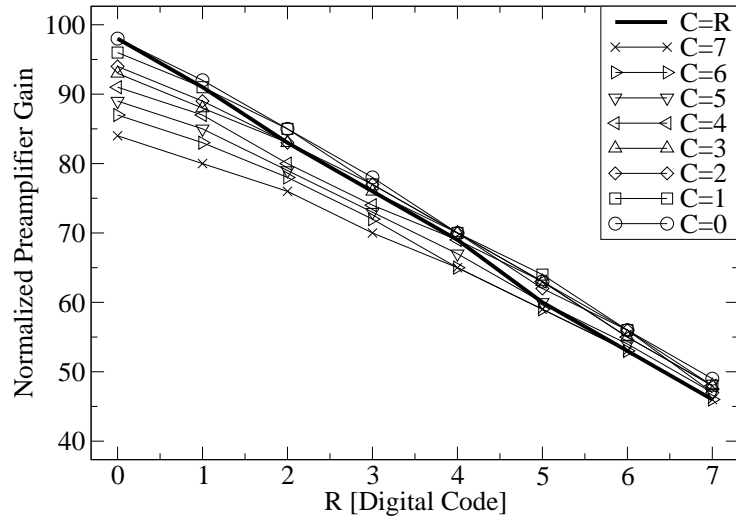


Fig. 9. Measurement results for adjustable gain of the preamplifier as a function of R and C binary D/A converter inputs.

environment. Two current mode D/As are taken for this simple case study.

Current mirroring D/As are based on an array of well matched unit current sources that are switched to the output. Three different schemes are possible depending on the implementation, namely the binary weighted (BWA), thermometer coded (TCA) and segmented architectures.

In BWA which is also the one presented in the previous section, every switch steers a current to the output which is twice as large as the next least significant bit. Also the digital input code itself directly controls the switches, that is, decoder logic is not needed. Hence, the layout can fit onto a small chip area; however, a relatively large DNL error is intrinsically associated with it. Even though, TCA has a better DC behavior, it requires more space as well as decoding logic. Segmentation could be used to benefit from the two architectures.

For an ideal comparison between BWA and TCA in terms of Integral Non-Linearity (INL) and Differential Non-Linearity (DNL), a C++ code was developed in ROOT environment[25]. N being the number of bits, 2^N unit current sources were created. The currents they provide were acquired randomly from a Gaussian distribution with a sigma of 0.02 separately for each unit current source. These sources were used to form both the D/As in BWA and TCA. In BWA, first 2^{N-1} unit current sources were summed to form the Most Significant Bit (MSB), then similarly the sum of next 2^{N-2} unit sources were used as the next bit to MSB and so on. Fig. 10 shows the simulation results. Coherent with the theoretical expectations[26], INL

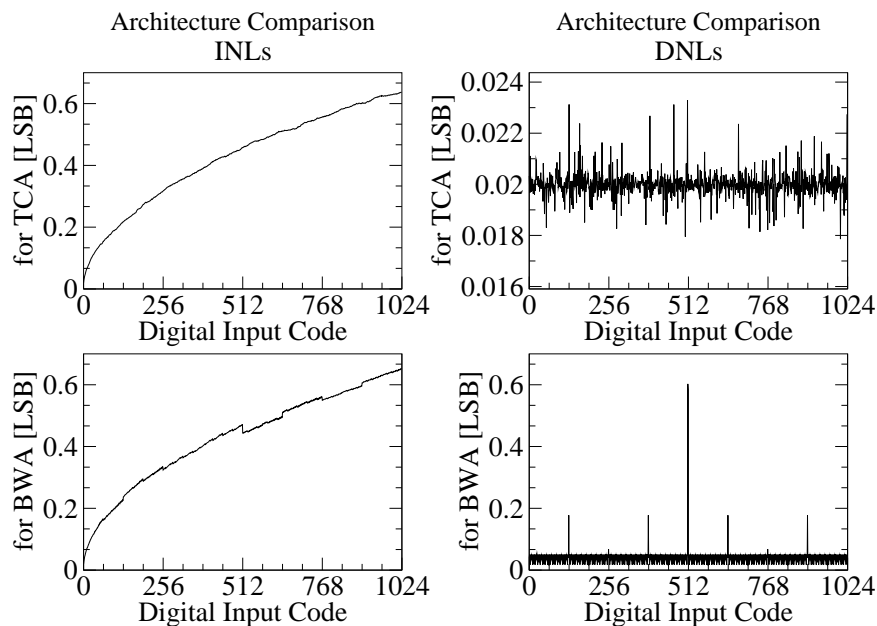


Fig. 10. RMS of 1000 Monte Carlo simulation results for $N=10$.

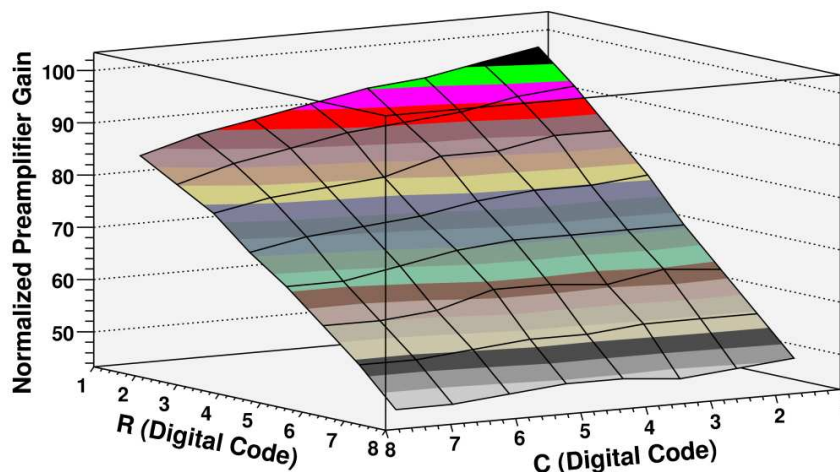


Fig. 11. Measurement results for adjustable gain of the preamplifier as a function of R and C binary D/A converter inputs.

variations for both architectures are almost identical and equal to $\sqrt{2N}\sigma = 32\sigma$. TCA represents a 32 times (σ) better DNL behavior than BWA does (32σ).

E. Test Results

Measurements showed good agreement with simulation results. Gain and the output pulse shape of the preamplifier is adjustable by controlling the values of capacitive and resistive components in the feedback path. These component values can be set either independently or in a correlated manner in order to preserve the shape of the output signal.

The gain of the preamplifier is a strong function of the resistor as seen in Fig. 9. Gray curves show the gain variation due to change in resistor while the capacitor value is preserved. In order to keep the signal with the optimum shape, the capacitor should be adjusted in such a way that the time constant remains the same. The black curve ($R=C$) shows the gain for which the digital inputs are equal, thus the output signal shape is maintained. As seen in Fig. 11, capacitor value has only a slight effect on the preamplifier gain. It is utilized to adjust the time constant but not the gain itself. An increase in the binary code for resistor must be accompanied by an increased capacitor code. Reverse logic is used internally in the chip to preserve the direction of the digital code change maintaining optimum signal shape.

Linearity of the preamplifier output is important for proper operation. Fig. 12 shows the measurement results. In the upper plot, circles represent the normalized preamplifier output values and the solid line is the linear fit. The nonlinearity is less than

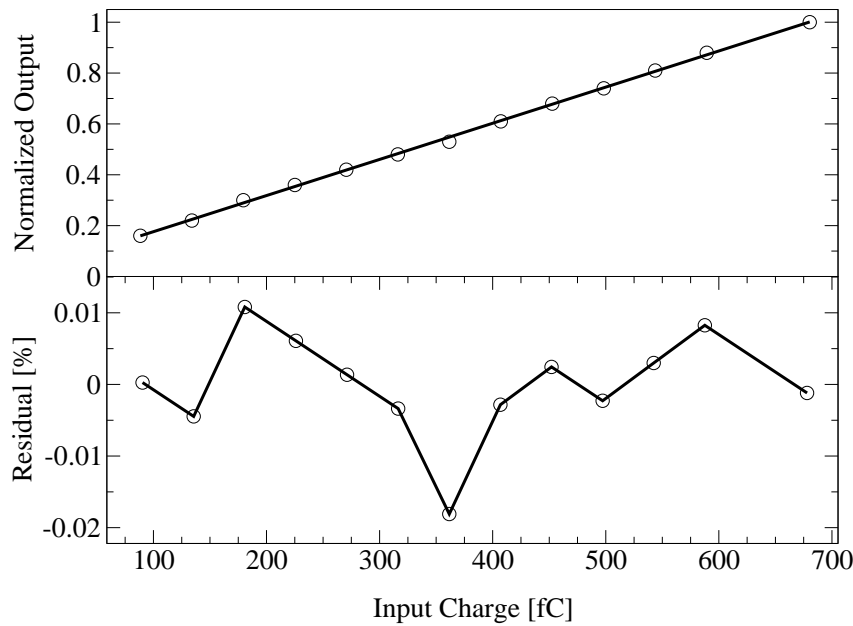


Fig. 12. Gain linearity of the preamplifier; measurement and linear fit (upper plot) and the difference between fit and measurement.

TABLE I
CMAD SPECIFICATIONS

Technology	0.35 μm
Number of Channels	8/Chip
Preamplifier Gain Range	0.4-1.2 mV/fC
Preamplifier Gain Resolution	0.08 mV/fC
Peaking Time	10 ns
Speed	>5 MHz/Ch
Chip Size	4.7x3.2 mm ²
Power (w/o LVDS Drivers)	26 mW

2%, as seen in residual between data and linear fit given at the bottom.

F. Summary for FE Electronics Study

- 1) Development : CMAD, a full custom ASIC for the upgrade of COMPASS RICH-1 detector system @ CERN-SPS
- 2) My contributions : Development of reference biasing circuits, the digital-to-analog converter, and I was involved partly in tests.
- 3) Publications : Conference records [x2], Full NIM paper (in progress) [x1]

III. CDR IN COMMUNICATION SYSTEMS

Clock and data recovery (CDR) is a critical function in high-speed transceivers. Such transceivers serve in many applications, including optical communications, backplane routing, and chip-to-chip interconnects. The data received in these systems are both asynchronous and noisy, requiring that a clock be extracted to allow synchronous operations. Furthermore, the data must be 'retimed' such that the jitter accumulated during transmission is removed. CDR circuits must satisfy stringent specifications defined by communication standards, posing difficult challenges to system and circuit designers.

In order to perform synchronous operations such as retiming and demultiplexing on random data, high-speed receivers must generate a clock. As illustrated in Fig. 14a, a clock recovery circuit senses the data and produces a periodic clock. A D flipflop (DFF) driven by the clock then retimes the data (i.e., it samples the noisy data), yielding an output with less jitter. As such, the flipflop is sometimes called a decision circuit. The clock generated in the circuit of Fig. 14a must satisfy three important conditions [27]:

- 1) It must have a frequency equal to the data rate; for example, a data rate of 10 Gb/s (each bit 100 ps wide) translates to a clock frequency of 10 GHz (with a period of 100 ps).
- 2) It must bear a certain phase relationship with respect to data, allowing optimum sampling of the bits by the clock; if the rising edges of the clock coincide with the midpoint of each bit, the sampling occurs farthest from the preceding and following data transitions, providing maximum margin for jitter and other timing uncertainties.

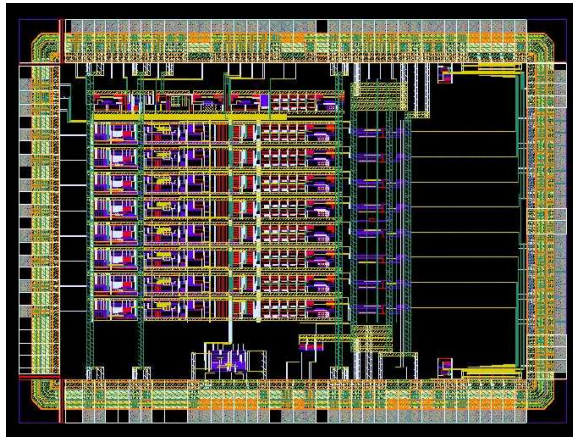


Fig. 13. CMAD chip layout.

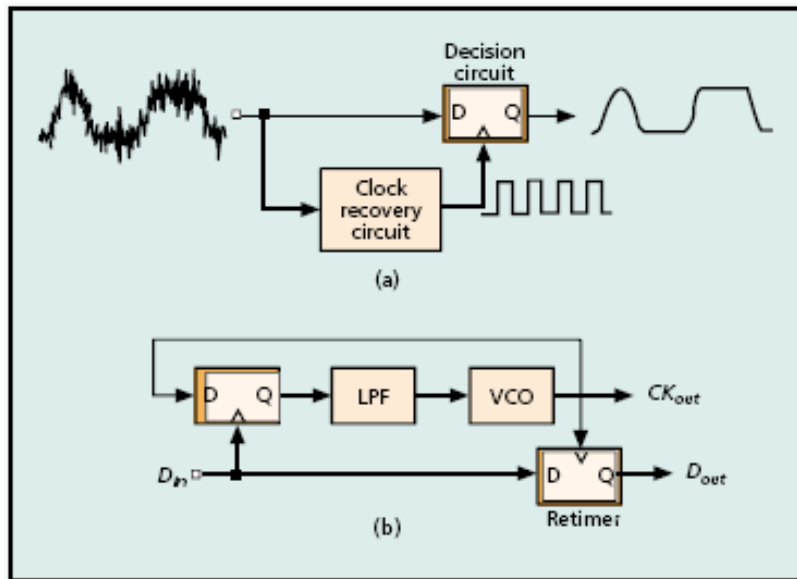


Fig. 14. a) The role of a CDR circuit in retiming data; b) an example of CDR implementation.

3) It must exhibit a small jitter since it is the principal contributor to the retimed data jitter.

As illustrated in Fig. 14a, to generate the clock waveform we employ a voltage-controlled oscillator (VCO), and to define its frequency and phase we phase-lock the VCO to the input data using a DFF operating as a phase detector (PD). The low-pass filter (LPF) suppresses ripple on the oscillator control line. Also, to retime the data, we add another DFF that is clocked by the VCO output. Note that the recovered clock, CK_{out} , drives the D input of the phase detector and the clock input of the retimer. The circuit of Fig. 14b operates as follows. Upon turnon, the DFF multiplies the edge-detected data by the VCO output, generating a beat that drives the VCO frequency toward the input bit rate. If the initial difference between the VCO frequency and the data rate is sufficiently small, the loop locks, establishing a well-defined phase relationship between D_{in} and CK_{out} . In fact, with the bang-bang characteristic provided by the DFF phase detector, the data edges settle around the zero-crossing points of the clock. Even for a slight phase error, the PD generates a large output, driving the loop toward lock.

Even though, this simple illustrative example could serve as a CDR, it suffers from a number of drawback which prevent its usage in real-world applications. First, the PD may produce full digital outputs for run lengths greater than one, thereby creating substantial ripple on the oscillator control voltage and hence jitter at the output. Second, since the PD samples the clock by the data, whereas the decision circuit samples the data by the clock, data retiming exhibits significant phase offset at high speeds. Typical flipflops display unequal delays from the D input to the output and from the clock input to the output. Thus, if, for example, the CK-to-Q delay is longer than the D-to-Q delay by dT , the PD locks such that the data leads the clock by dT , sampling the clock closer to the zero crossing after the data experiences the intrinsic delay of the PD. The VCO output suffers from even more delay as it propagates through the decision circuit, sampling the data far from the middle of the

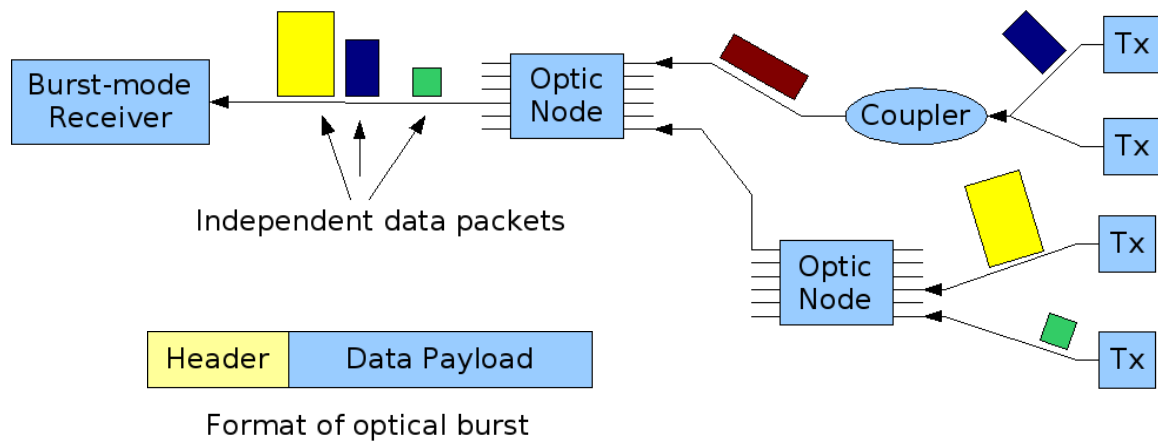


Fig. 15. A burst-mode network

eye. In other words, if the difference between the CK-to-Q and D-to-Q delays is equal to dT , the retiming suffers from a skew of $2dT$. The third drawback of the simple CDR architecture of Fig. 14b relates to the feedthrough of data to the VCO output through both flipflops. The output phase is disturbed on arrival of each data transition, requiring that the VCO be followed by a buffer stage providing significant reverse isolation.

A. Burst-Mode CDR

In HEP applications the detector systems are supposed to operate fast and well organized. An experiment controller sends/receives data to/from various types of sub-systems and organizes their activity. For this purpose, a bursty data stream could be used. This means that the data packets coming/going to/from sub-systems can have different signal height, frequency, phase and noise, thus requiring a burst-mode capable transceiver design as shown in Fig. 15.

Burst-Mode communication relies on very fast acquisition circuitry to achieve low network latency. If the data stream is bursty, the receiver must be able to synchronize with the data instantaneously to maintain reliable communication. For Burst-mode communication, conventional clock recovery (CR) methods based on narrow-band phase-locked loops (PLLs), such as the ones designed for SONET applications, are not applicable. PLL-based CR circuits in SONET have stringent jitter transfer specifications to avoid jitter accumulation. In addition, they are required to tolerate long sequences of identical bits. These constraints impose a narrow-band PLL that will have long acquisition time [28].

B. Motivation of Burst-CDR for GBT13

The current TTC (Timing Trigger and Control) system[?] is an optical broadcast network that will be used for fast timing and slow control distribution at the CERN-LHC. The system provides for the broadcast of fast timing signals through all the transmission stages from the RF generators of the LHC machine to the outputs of the timing receiver the TTCrx. A detailed overview of the TTCrx operation is given on the ASICs reference manual[?] that can be found on the TTC system web site[?].

The TTC system users experience revealed some restrictive features that in most cases resulted from technological limitations at the time of the development of the system. These days, the perspective of an upgrade of the LHC and the common availability of deep sub-micron technologies can lead to the development of an extended functionality timing, trigger and control system requiring the development of a new timing receiver, the GBT13.

Some of the major drawbacks that were identified on the TTC system and/or on the TTCrx are:

- 1) Transmission of a single trigger type;
- 2) Several bunch crossing periods are required to transmit broadcast commands and slow control data;
- 3) The system is unidirectional. This required the late addition of an I2C network in order to control the TTCrx, necessitating the presence of an additional control path;
- 4) Although broadcast commands and slow control data are protected by error correction codes the trigger data is not;
- 5) If not synchronized with the TTC signal source the TTCrx generates a random clock frequency. This is undesirable for purposes of system development and testing.

The drawbacks mentioned in points 1) and 2) can be avoided by increasing the transmission data rate that in the current system is 80 Mbit/s. This will allow sending during a single bunch crossing interval complex trigger information, broadcast commands as well as individually addressed commands and data. Addition of a return path will address point 3) and would allow the implementation of an efficient monitoring system not only of the state of the TTC system itself but of the detectors electronics. Such a system resembles very much a bidirectional data link with added features to implement the synchronization

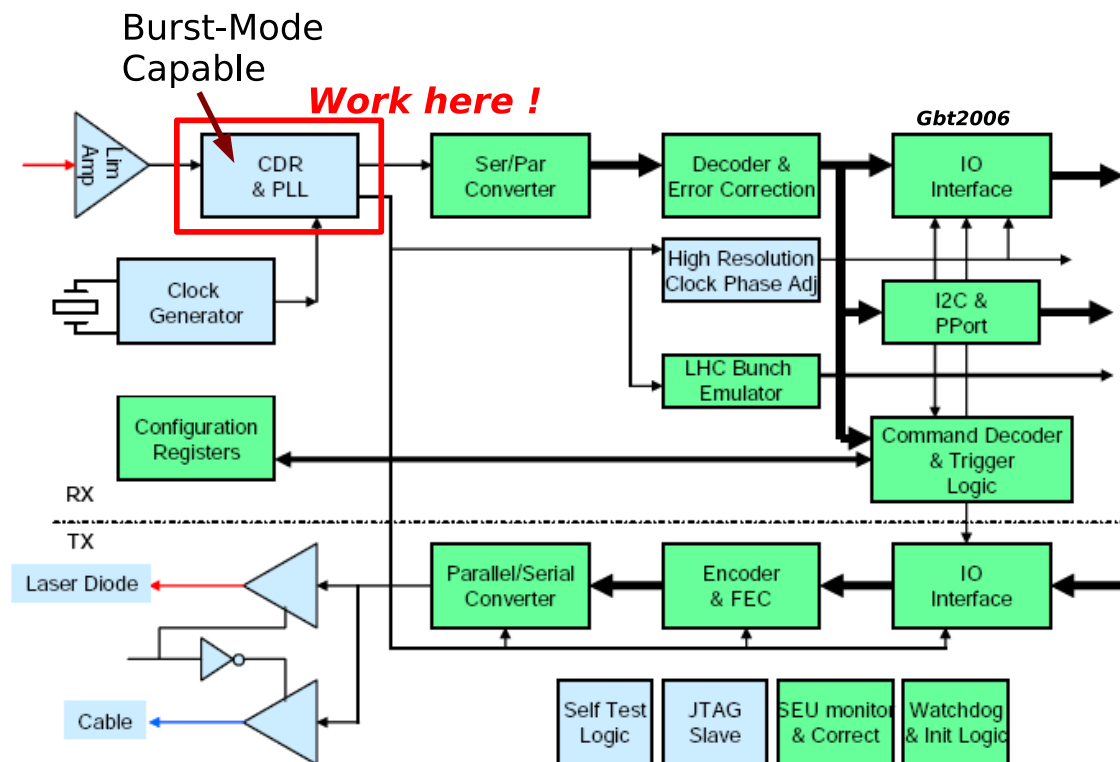


Fig. 16. Simplified GBT architecture

of the detectors. It is thus conceivable to implement a bidirectional link that could work either as a general purpose data link or as a dedicated timing trigger and control link. To implement such a scheme the receiver and transmitter components must be radiation hard and tolerant to single event upsets. The use of error correction codes for data transmission must be considered.

Fig 16 shows the proposed full GBT architecture and Fig. 17 shows a network configuration in which GBT transceivers would be used.

C. Proposed Architectures

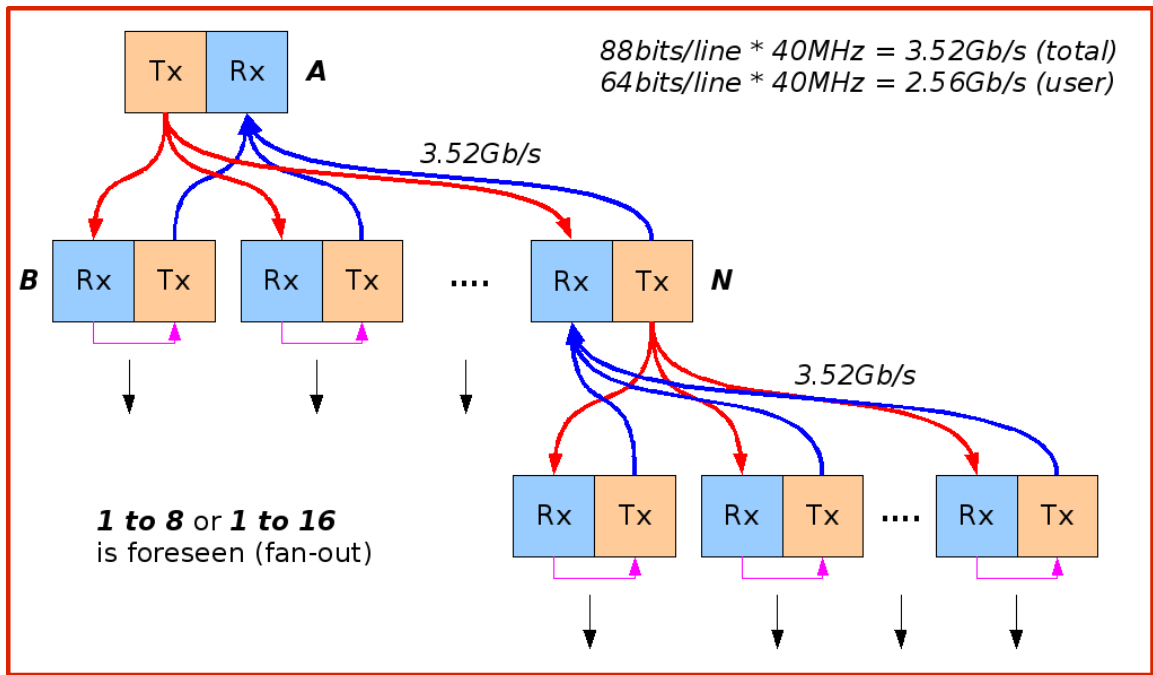
If the clock error and burst length are limited then a variable delay can be used to lock the data to a local clock. As seen in Fig. 18, FLL is always locked, burst-mode receiver knows the frequency but not the phase. Delaying the data is the fastest solution in this case; phase alignment is instantaneous (we have 8 bits as preamble for GBT, though) Either CK or Vctrl must connect the two blocks. Connection between the two loops is FREQ. This design fails in continuous mode if FREQ and Din has different "frequencies" (wander). Architecture seen in Fig. 18 is perfect for burst-mode but we can not use it both for burst and continuous stream because the delay is always limited and the error accumulates indefinitely after a certain time period.

In Fig. 19, another design idea is shown. Instead, an analog value is the connection between two blocks. At every data transition, jitter is reset. We have 5 CIBs since we have a line coding scheme in GBT. Jitter accumulation is limited to 5 bits in the worst case. VCOs can be identical enough with proper layout. This is suitable for both types of communication (burst and continuous). Implemented in a similar technology, with 30ps delay in Gating Circuit @ 10Gb/s. Either we must have 2 VCOs and Din passes through one block or we must have 1 VCO and Din goes to both (see Fig. 21).

Fig. 20 shows the instantaneous lock to data at 10Gb/s speeds.

Fig. 21 shows a complete CDR architecture. d/dt changes the time constant of the LPF, it serves as the memory for the delay line. Red line on the figure is the reference frequency/phase which locks to Din slowly in continuous mode, which Din locks to it instantaneously in burst mode. In this architecture not even a single bit is lost independent of the mode : Right block can accept hundreds of Kbytes of data and this gives PLL enough time to take over.

In Fig. 22 the final CDR architecture is shown. This is the circuit which combines both functionality : i) When Din is burst-mode, it accepts the data, phase alignment is instant, each data transition resets phase error with a worst case accumulation of 5 consecutive identical bits, ii) Can be designed such that it can accept Kbytes of data, providing Fine Loop enough time to take over (we have 11Bytes in GBT preamble, though). It can continue operating even after Fine Loop locks. When Din is continuous-mode, same thing happens. Exactly the same circuit operates in two different modes.



Second configuration

Fig. 17. A network configuration with GBTs in use

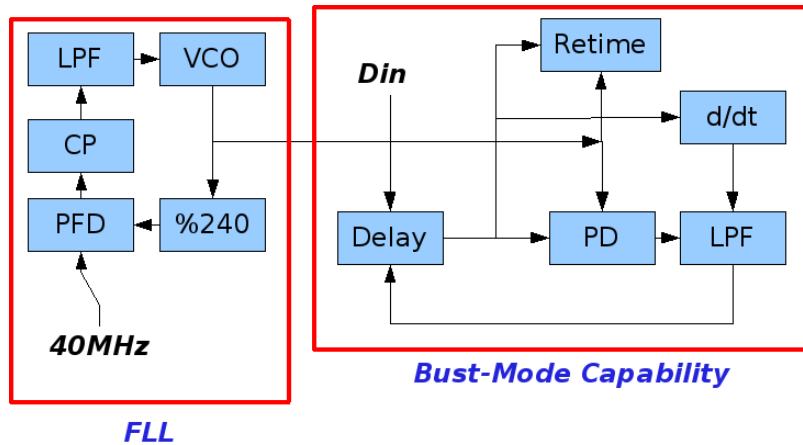


Fig. 18. A CDR architecture

Here the D-FF is a double edge triggered flip-flop and the G-VCO keeps its output level as it is if the gating signal is low. The Verilog HDL model of this architecture is also developed for further simulations.

D. Analysis for PLL on Which The CDRs Depend

Fig 23 shows a charge pump PLL example on which the analysis presented in this brief will be based. Fig. 24 shows the behavioural model of the CP-PLL shown in Fig. 23. Fig. 25 shows the basic equations for design parameters of a PLL. Non-idealities result in divergencies from the expected behaviour. Fig. 26 shows the effect of meta-stability in the phase detector block of a CDR whereas Fig. 27 shows the high level jitter transfer model in PLL based loops. Another non-ideality is the VCO phase noise jitter generation as shown in Fig. 28.

Jitter tolerance and transfer model parameters could conflict with CDR loop parameters and both models can be further "updated" and become complicated. Parameters in these models can be optimized with Evolutionary Algorithms (EA) : A good example to Multi Objective Optimization Problem. Even though, transistor level circuits can be designed and optimized by EAs, we will not have time for this but we could have time for the EAs.

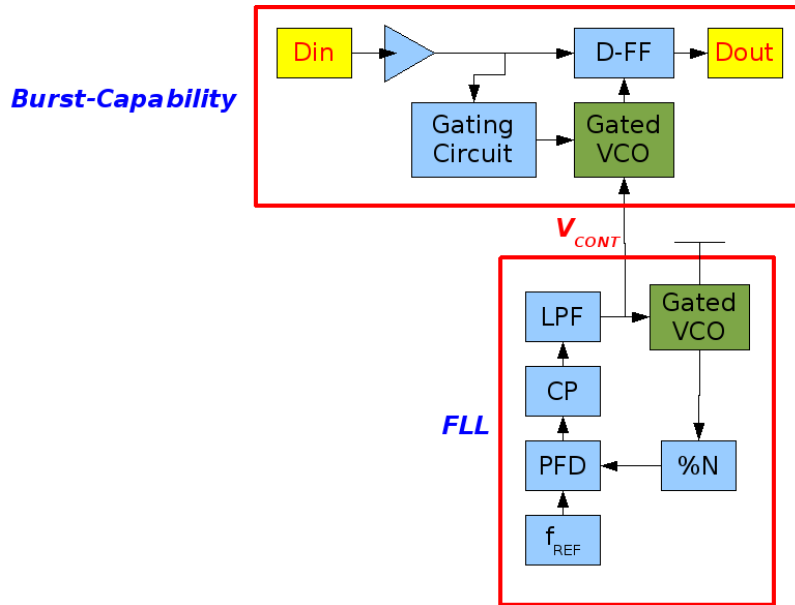


Fig. 19. A CDR architecture

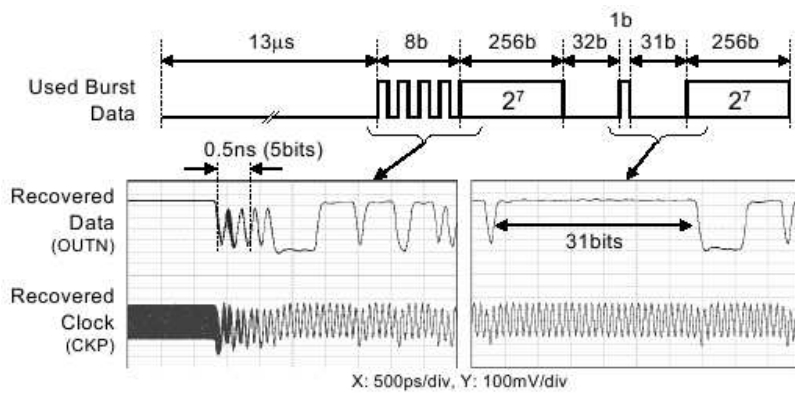


Fig. 20. Instantaneous locking @10Gb/s

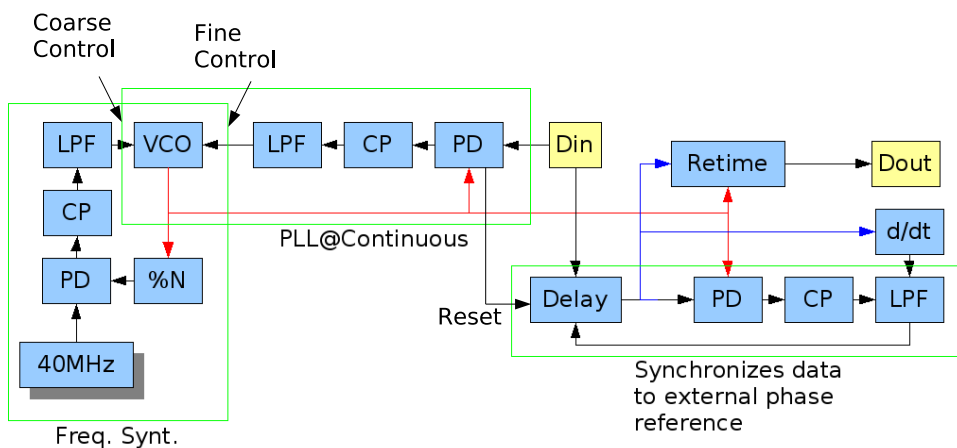


Fig. 21. A CDR architecture.

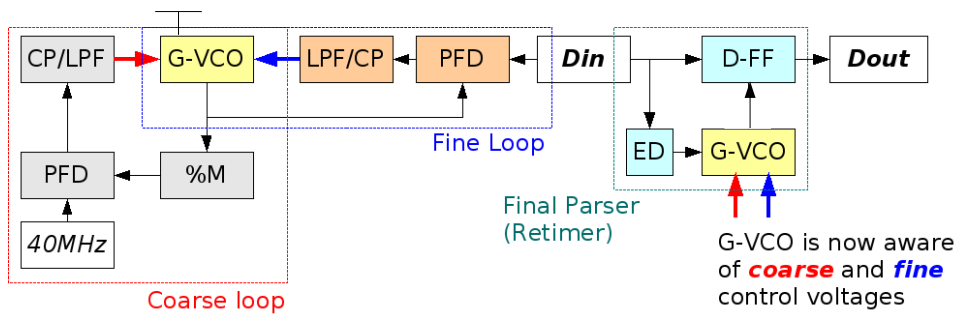


Fig. 22. The final proposed CDR architecture.

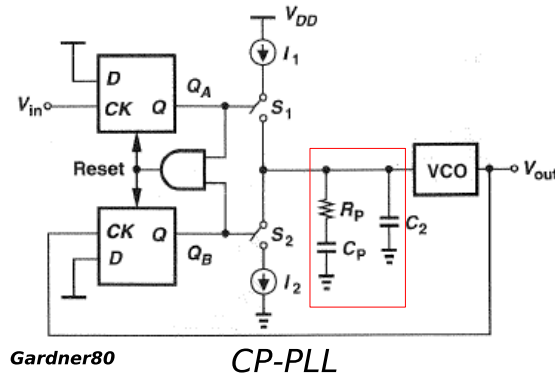


Fig. 23. Charge pump phase locked loop.

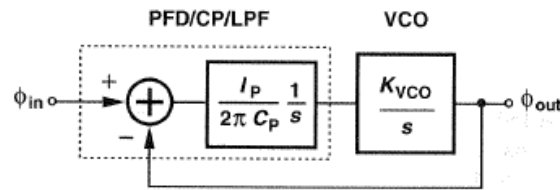


Fig. 24. Charge pump phase locked loop behavioural model.

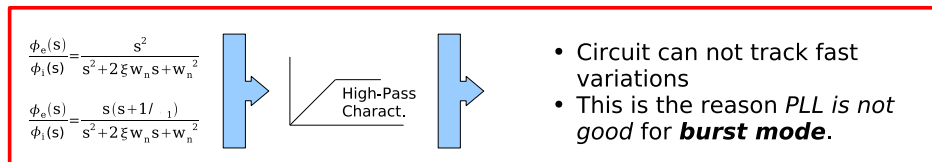
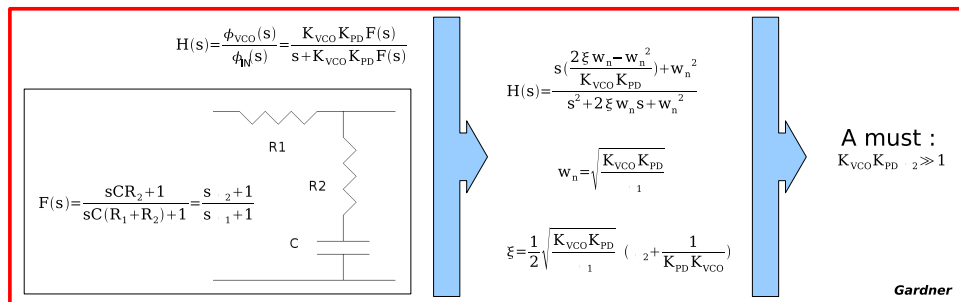
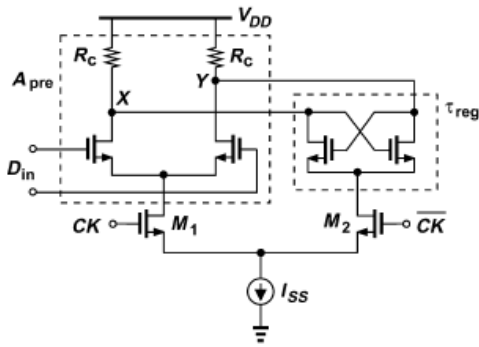


Fig. 25. Charge pump phase locked loop equations.



- D_{in} causes X and Y to develop a potential difference within "**sampling time**" and **regenerative pair** keeps these values

- **When $CK=1$** , X and Y goes away from each other
- **When $CK=0$** , regenerative pair steers current according to the potential of X and Y
- If CK is set to 0 "**before**" complete switching of X and Y, regenerative pair "**confuses**"

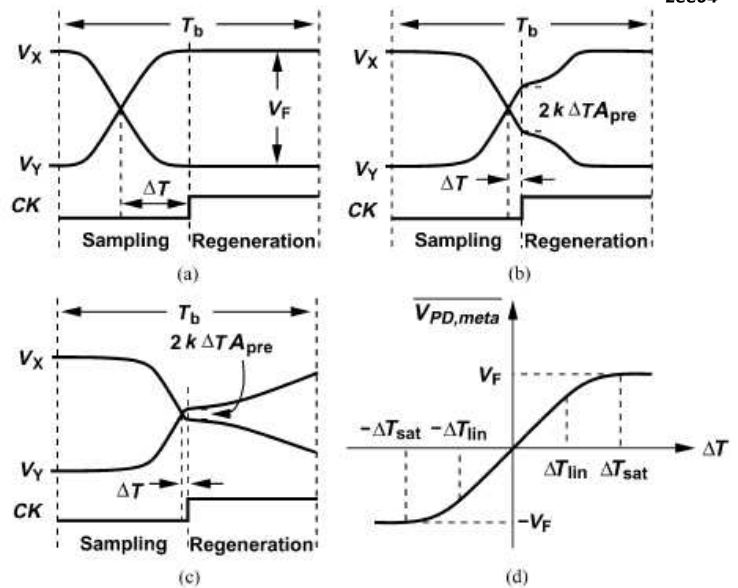
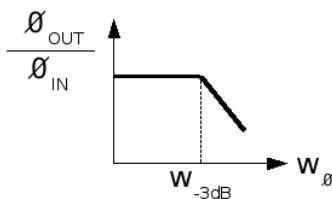
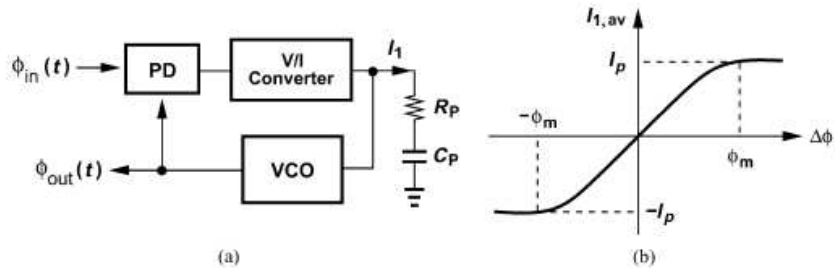


Fig. 26. Small Phase Error - Effect of Metastability

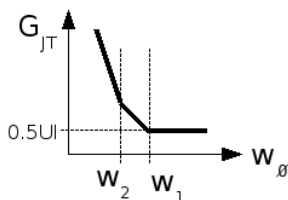
Based on the model in the figure, jitter characteristics will be examined.



$$w_{-3dB} = \frac{\pi K_{VCO} I_P R_P}{2 \phi_{IN}}$$

Jitter Transfer

(Gain peaking < 0.1dB, $w = F_b/1250$, ITU Standard)



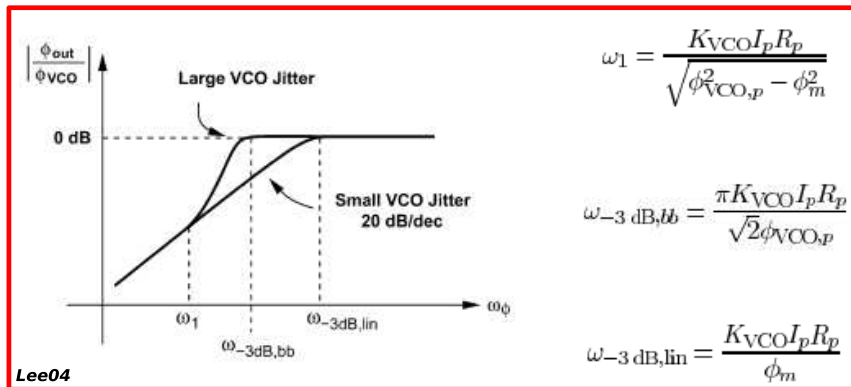
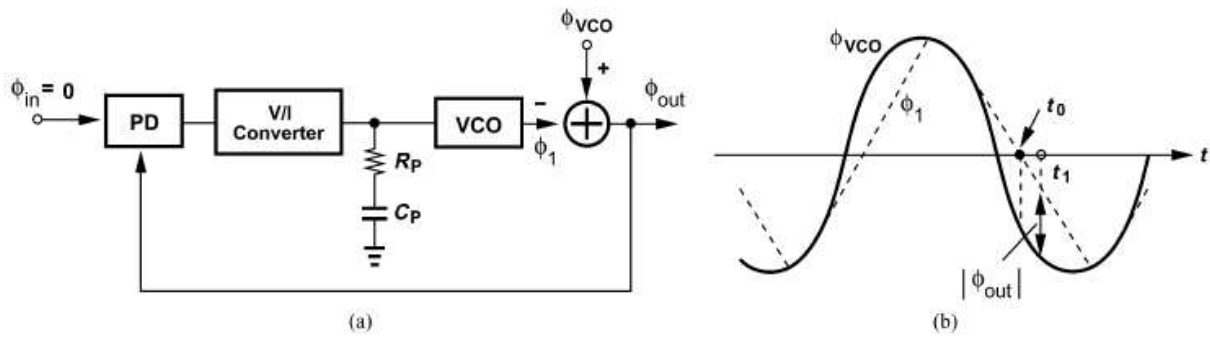
$$w_1 = \frac{K_{VCO} I_P R_P}{2}$$

High Freq. Jitter Tolerance

$$w_2 = \frac{0.63 \pi}{R_P C_P}$$

Low Freq. Jitter Tolerance

Fig. 27. High level jitter model



- (a) VCO phase noise addition, (b) effect of slewing because of VCO jitter
- VCO jitter transfer function and the “corners”

Fig. 28. VCO Phase Noise Jitter Generation

E. Summary for Burst-CDR Study

- 1) Development Target : Burst-Mode capable Gb/s class Clock and Data Recovery (CDR) chip of Giga Bit Transceiver (GBT) for S-LHC @ CERN (in progress)
- 2) My contributions : would be modeling, designing, implementing, and testing of burstmode capability building block of the full CDR
- 3) Target Publications : Conference records [?], IEEE Full paper [?]

IV. CONCLUSION

An overview of detector FE electronics and burst-mode capable Clock and Data Recovery (Burst-CDR) architectures for transceivers intended for nuclear and High Energy Physics experiments were considered. Proposed architectures were given in steps leading to those structures. Models and the optimization parameters were presented.

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