Front-End Electronics in 0.13μm CMOS Technology with 100ps Time Resolution Capability for Silicon Pixel Radiation Detector Gigatracker in NA62 Experiment

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Outline

- NA62 experiment
- GTK detector
- Timing techniques
- Two prototypes:
  - Architectures
  - Test results
Context of the Work

- NA62 experiment at the CERN SPS accelerator to measure $|V_{td}|$ in CKM (Cabibbo-Kobayashi-Maskawa) matrix
- $K^+ \rightarrow \pi^+ \nu \bar{\nu}$
- 80 events with a branching ratio of $10^{-10}$
- $8 \cdot 10^8$ particles/s, 75 GeV/c
Physics Motivations

\[ \text{BR}(K^+ \rightarrow \pi^+ \nu \bar{\nu}) = 6r_k \text{BR}(K^+ \rightarrow \pi^0 e^+ \nu) \]
\[ \frac{|G_i|}{G_F^2 |V_{us}|^2} \]

\[ G_i = \alpha G_F \frac{[V^*_{ts} V_{td} X(x) + V^*_{cs} V_{cd} X_{NL}]}{2\pi \sin^2\Theta_W} \]

\[ V_{td} \text{ theoretical error of } \sim 5-7\% \]
# Background Rejection (1)

<table>
<thead>
<tr>
<th>Decay mode</th>
<th>BR</th>
<th>Background rejection</th>
</tr>
</thead>
<tbody>
<tr>
<td>$K^+ \rightarrow \mu^+\nu$</td>
<td>63%</td>
<td>$\mu$ PID, kinematics</td>
</tr>
<tr>
<td>$K^+ \rightarrow \pi^+\pi^0$</td>
<td>21%</td>
<td>$\gamma$ veto, kinematics</td>
</tr>
<tr>
<td>$K^+ \rightarrow \pi^+\pi^+\pi^-$</td>
<td>6%</td>
<td>charged particle veto, kinematics</td>
</tr>
<tr>
<td>$K^+ \rightarrow \pi^+\pi^0\pi^0$</td>
<td>2%</td>
<td>$\gamma$ veto, kinematics</td>
</tr>
<tr>
<td>$K^+ \rightarrow \pi^0\mu^+\nu$</td>
<td>3%</td>
<td>$\gamma$ veto, $\mu$ PID</td>
</tr>
<tr>
<td>$K^+ \rightarrow \pi^0e^+\nu$</td>
<td>5%</td>
<td>$\gamma$ veto, $E/p$</td>
</tr>
</tbody>
</table>
• Region I: \( 0 < m_{\text{miss}}^2 < m_{\pi^0}^2 - (\Delta m)^2 \)

• Region II: \( m_{\pi^0}^2 + (\Delta m)^2 < m_{\text{miss}}^2 < \min[m_{\text{miss}}^2 (\pi^+\pi^+\pi^-)] \)
Background Rejection (3)

\[ m^2_{\text{miss}} = m^2_K (1 - \frac{|P_\pi|}{|P_K|}) + m^2_\pi (1 - \frac{|P_K|}{|P_\pi|}) - \frac{|P_K||P_\pi|\theta^2_{\pi K}}{|P_K||P_\pi|} \]

- \( \Delta|P_K|/|P_K| \sim 0.3\%, |P_K| = 75 \text{ GeV} \)
- \( \Delta|P_\pi|/|P_\pi| \sim 1\% \text{ at 30 GeV} \)
- \( \Delta\theta_{\pi K} \sim 50-60 \mu\text{rad} \)
- \( (\Delta m^2_{\text{miss}}) \sim 8 \times 10^{-3} \text{ GeV}^2/c^4 \)

GTK
- 300\(\mu\)m x 300\(\mu\)m pixel
- \( \sim 100 \text{ ps time} \)
  resolution due to high particle rate (60MHz/cm^2)
Experimental Setup

- P and t detection
- $\gamma$ veto
- PID

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ASIC

Application Specific Integrated Circuit

- Implementation of custom functions
- Minimization of cost, size and power consumption
- Man power: 5-10 man-years
- 50,000 $ per 10mm²
CMOS technology (1)

CMOS inverter

The gate length defines the technology node

Electron Micrograph of CMOS FET Cross Section

The gate length defines the technology node
CMOS technology (2)

Scaling consists in changing the physical parameters of a MOSFET so that the scaled device will have similar behavior.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Scaling Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device dimension (Width, Lenght, oxide thickness)</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Power supply and voltages</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Doping density</td>
<td>$\kappa$</td>
</tr>
<tr>
<td>Speed</td>
<td>$\kappa$</td>
</tr>
<tr>
<td>Devices density</td>
<td>$\kappa^2$</td>
</tr>
<tr>
<td>Power density</td>
<td>$1$</td>
</tr>
</tbody>
</table>

Issues:
- Parasitic effects
- Quantum mechanical tunneling currents
- Non-scaling of Threshold voltage
- Random dopant fluctuation
Substrate Noise
\[ \sigma_t = \frac{\sigma_n}{\frac{dV}{dt}} \]
signals with constant rising time and different amplitudes

time walk error
ToT: time walk correction is based on an algorithm derived from the correlation between the pulse width and the experienced time walk. In this case two time measurements (rising and falling edge) are performed.
Timing Techniques: Time Walk (3)

\[ y(t) = \frac{At}{t_p} \]
\[ y(t-t_d) = fy(t) \]
\[ A(t-t_d) = \frac{fAt}{t_p} \]
\[ t = \frac{t_d}{(1-f)} \]

Approximation: triangular signal

Hypothesis: crossing point always on the linear rising portion of the input signal
- 3 GTK stations
- One silicon sensor (60mmx27mmx200µm)
- 2x5 read-out chips
- Carbon cooling/support plate with high heat conduction
- Support and alignment structure outside the beam area
• Time resolution of 200ps (rms) on the single station (3 stations → $200/\sqrt{3}=115$ps): jitter, digitization and time walk

• Efficiency > 99%: 1fC threshold

• Dead time < 1%: max event rate of 150kHz/ch

• Power consumption < 1mW/ch: 48bits × 800part/s = 38.4 Gbits/s for each station

• Radiation tolerance: SEU and integral dose deterioration of the sensor
EoC Solution

- Leading edge comparator: offline correction of time walk
- EoC approach: 40 TDCs

320MHz clock
TDC per Pixel Solution (1)

- CFD: online correction of time walk
- local approach: 1800 TDCs
TDC per Pixel Solution (2)

Clock (6.25ns)

time-stamp
discriminator output

ramp

coarse time (10 bit)

fine time (8 bit)

$V_{\text{TAC}}$

ADC
Conversion time up to $1.2\mu s$ with 8-bit Wilkinson ADC: local derandomization
Charge/discharge currents matching: generators of the same type and 1:16 mirroring ratio
(4x6.25ns/256=98ps)
- 70ps rms at laser test
- 200ps rms at beam test
- Statistical fluctuations in charge release
- Pixel border effects
TDC per Pixel Demonstrator

- 2 test pixels
- EoC logic
- Column 0 – 15 cells
- Column 1 – 45 cells
- Column 2 – 45 cells

5 mm

3 mm

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Pixel Layout

- CFD filter
- TDC
- Preamplifier

Digital section: 300 µm

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10^6 random test pulses to the 7-bits TDC:
\[ N_{th} = \frac{10^6}{2^7} \]

\[ \rightarrow -0.5 < \text{DNL}(i) = \frac{N_{exp}(i) - N_{th}(i)}{N_{th}(i)} < 0.5 \]

\[ \rightarrow -1 < \text{INL}(i) = \sum_{i=0}^{k} \text{DNL}(i) < 1 \]
Good linearity

Good uniformity

TDC Linearity (3)
TDC Linearity (4)

\[
t = t_c + (2T_{ck} - t_f) \text{ if } t_f \leq 2T_{ck}
\]

\[
t = t_c + (3T_{ck} - t_f) \text{ if } t_f > 2T_{ck}
\]
TDC Linearity (5)
- ~ 200ps time bin at 80 MHz
- 400ps peak-to-peak error due to substrate noise
TDC Linearity (7)

PSRR to be optimized
92ps (rms) time resolution measured at the oscilloscope on the test pixel without the clock
Time walk of a matrix pixel vs Test Pulse delay

CFD (2)
CFD (3)
CFD (4)

Baseline (mV) vs. t/Tck

- Yellow line: binary mode
- Blue line: gray mode
Jitter

bin  i-1  i  i+1

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Conclusions and Outlook

- Two ASICs produced in the R&D of GTK for NA62 experiment
- EoC prototype gave 70ps (rms) in laser tests and 200ps (rms) at the beam test
- One more prototype required for TDC per pixel solution
- Other applications for TDC per pixel: medical imaging, silicon pixel photomultipliers