Integrated Circuit Design for Time-of-Flight PET

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LIP - Laboratorio de Instrumentacao e Fisica Experimental de Particulas
Unito - Universita degli Studi di Torino
INFN - Istituto Nazionale di Fisica Nucleare sez. Torino

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Torino Graduate School in Physics and Astrophysics
XXVI cycle Seminar
February 20 2013, Turin, Italy
1. Time-of-Flight PET: Motivation and Framework

2. Choice of the chip architecture

3. The 64-channel TOFPET ASIC
   - Operation with SiPMs
   - Floorplan and Packaging
   - Characterization

4. Summary and Outlook
Outline

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4. Summary and Outlook
An injected radiopharmaceutical undergoes a $\beta^+$ decay, from which a positron is created. Its annihilation in the vicinity of the tumourous tissue produces a pair of high-energy photons flying back-to-back. The quasi-simultaneous detection of the two $\gamma$ rays describes a LOR. With multiple LORs, a slice of the image is built. Reconstruction of different angle projections is used to retrieve a 3D image.
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Basics of PET - the planar detector heads case study

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Motivation for Time-of-Flight measurements in PET

A 200 ps coincidence resolving time (CRT) confines the annihilation coordinate to a 3 cm segment along the LOR.

This measurement can identify, with an error $\Delta x = \Delta t \cdot \frac{c}{2}$, the position of the annihilation along the chord that defines the travel path of the back-to-back photons.

- spatial resolution is the same
- background rejection is significantly improved

Consequently achieving:

- Higher SNR of the reconstructed image,
- Shorter exam time, or
- Reduced injected dose of radiopharmaceutical
Combined TOF-PET (200 ps time resolution), ultrasound imaging and endoscopic biopsy

PET components:
- dSiPM/crystal endoscopic probe
- aSiPM/crystal external plate
Readout ICs for Time-of-Flight PET

Combined **TOF-PET (200 ps coincidence resolving time resolution)**, ultrasound imaging and endoscopic biopsy

- **Extraction of TOF information:** Need to trigger the time-of-arrival of the first photoelectron(s) to reduce the effect of the scintillation light statistics
- **Endoscopic probe PET:** crystals and SPAD array (TU Delft)
- **External PET plate:** crystals, SiPMs and custom ICs:
  - **STiC2 (Univ. Heidelberg):** digital-based TDC
  - **TOFPET-ASIC (LIP/INFN):** analogue-based TDC

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Technology Overview - SiPM, LYSO crystals

- Solid-state photodiodes array (operating in Geiger mode)
- Low-form factor, compact and robust: highly dense matrix
- Suitable to MRI: immune to magnetic fields (short carrier path)
- Very high gain ($10^5$ to $10^6$), comparable to that of PMTs

- Density 7.4 g.cm$^{-3}$
- Light Yield 27000 photons/MeV
- Emission peak 420 nm
- Time Constant 40ns
# Features of an ASIC for SiPM readout in PET applications

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<td>Clock frequency</td>
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How these specs impact the choice of the readout chip architecture?
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4. Summary and Outlook
Time pick-off method

- **Sampling Techniques**
  - Potentially best time and energy resolution
  - Complex circuitry for such high dynamic range (100 fC - 300 pC)

- **Threshold Techniques**
  - **Constant fraction**
    - Reduces time-walk, potential better time resolution
    - Difficult to implement if signal shape is unknown
    - Difficult to implement for high dynamic ranges
  - **Single threshold**
    - Easiest circuit topology
    - No hit rejection
    - Excessive jitter for ToT measure?
  - **Multiple threshold**
    - Easy circuit topology
    - Low-threshold for good timing
    - High-threshold for dark count rejection and ToT measurement
    - Energy measurement can be used for time-walk correction
    - Low jitter requires very fast and low-noise front-end
Time-to-digital Conversion

Simpler approach: count the cycles of a reference clock of the measurement interval. Need more accuracy? Increase clock frequency. Reasonable? :

- power budget..
- feasibility. Maximum frequency around 5GHz for deep sub-micron CMOS (max 200ps accuracy).

**Digital-based TDCs**
The clock is asynchronously subdivided (reference clock interpolation). Multiple phases of CLK are obtained with a chain of delay elements (susceptible to PVT variations) or a DLL.

**Analogue-based TDCs**
An analogue integrator performs time-to-voltage conversion, which can be then digitized by an ADC. The minimum resolving time $\Delta t$ is dependent on the maximum time to be measured ($DR$) and the number of bits ($N$) of the ADC. $DR = 2^N \cdot \Delta t$

Analogue interpolation seems to be more suitable for low power, compared to the more power-hungry DLL-based TDCs.
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Analogue-based TDC

For short measurement intervals, the analogue integrator can be devised with a current source charging a capacitor during the measurement interval (extensive calibration is needed, non-linearity due to finite $Z_{out}$ of the current source, ..)

Possible way out? A dual-slope analog-to-time interpolation:

- A ramp is charged by an integration constant $\tau_k$, and discharged with $\tau_k/n$
- DR is multiplied by $n + 1$: "time amplification"
- Hence, time resolution can be enhanced just by increasing $n$
- Digitally-assisted analogue blocks to finely calibrate the time binning

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Overview of the chip architecture

The TOFPET ASIC consists of a 64-channel analogue block, calibration circuitry, Golden-reference and Bias generators and a global controller.

- LVDS 10 MHz SPI configuration link for bias/channel setting
- LVDS 160-640 Mbps data output interface
- On-chip DACs and reference generators
Overview of the channel architecture

- **Time** and **charge** measurements with independent TDCs
- TDC time binning **50 ps**
- Charge measured with Time-over-threshold
- Typ. power consumption is **7mW p/channel** *(trigger 0.5 p.e. w/ SNR > 23dB for 9 mm² MPPC, 40 KHz event rate, 1MHz DCR)*
Front-End

- Low-Zin pre-amplifier, 2 independent TIA branches for **Timing** and **Energy** triggers
- Fine adjustment of the HV bias (6-bit over 500mV range) of the SiPM
- Selectable shaping function for Vout_E to avoid re-triggering and correct eventual loss of ToT vs. Qin monotonicity
- Selectable delay line for dark count filtering
- Usable for p-type or n-type (hole, electron collection) devices
Time-to-Digital Converter

Analogue TDC with 50 ps time binning - based on Time-to-Amplitude Conversion [Stevens89, Rivetti09]

- TDC Control: switching, hit validation, buffer allocation, data reg.
- Time stamp: 10-bit master clock count + Fine time measurement
Geant generated SiPM+LYSO data

Simulation of the whole channel (TDC CTRL simulated at transistor level); input is a test vector with data generated from GAMOS/c++ routines.\(^1\)

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TDC operation for a valid event

\[ \text{ToT (energy meas)} = t_2 - t_0 \]
Floorplan of the 64-channel mixed-mode chip

- CMOS 130nm $25 \text{mm}^2$ 64-channel ASIC
- Highlight shows the allocated area for bias and calibration circuitry.
- One pad-free edge to allow abutting two twin chips into a 128-channel BGA package.
Packaging of a 128-channel SiP

- The TOFPET ASIC has one pad-free edge
- That allows a second (rotated) chip to be abutted
- The compact 7x7 mm SiP can be packaged into a BGA
Packaging of a 128-channel SiP

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BGA package for the 128-channel assembly

View of the BGA ballout (17x17x1.70 mm 4 Layers PBGA 400) for the 128-channel assembly (left) and corner detail of the package substrate (right):
Test Setup @Lisbon (PT)

- Test setup for 128-channel SiP - Characterization ongoing
Test Setup @Turin (IT)

- Test setup for 64-channel board bonded chip - Characterization ongoing
Preliminary Results - ToT trend (TDC not yet used)

ToT (ns) vs. Input Charge (p. d. u. ~ 100 fC .. 180 pC)
(sweep of internal calib on channel 0) - without TDC fine time measurement

VthT@3pe, high VthE, sweep of the 6-bit range of the calibration test pulse - average of 50 pulses per point, 2 frames period - 80 MHz
Preliminary Results - TDC sampling noise

- Chip CLK_OUT clocks an external FPGA (160 MHz)
- 1000 FPGA’s sync’ed test pulse are fed to the input of the TDC, in test mode
- Fine time measurement variation (50 ps bin) is due to the jitter of the test pulse and the TDC quantization

\[ TP\ \text{jitter} + \ TDC\ \text{noise} < 0.5 \ \text{LSB}, \] using the id of the TDC buffer.
Preliminary Results - Front End Jitter

- 1000 FPGA’s sync’ed test pulse are fed to the front-end input, chip works in acquisition mode. Inputs not connected to a sensor.
- Fine time measurement variation (low-Vth) is due to the jitter of the front-end, summed to that of the test pulse and the TDC quantization.
- TOT fine time measurement affected by limited slope of the emulated 40 ns decay of the calibration pulse.

\[
\text{TP jitter} + \text{FE jitter} + \text{TDC noise} \approx 60 \text{ ps FWHM,}
\]

using the id of the TDC buffer.
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Summary and Outlook

- Low power (7mW p/channel), low noise readout IC for SiPMs
- 64-channel ASIC tape-out July 2012, internal CERN Engineering Run
- 112 chips p/wafer, 4 wafers ready
- Compact 17x17 mm 128-channel BGA package
- Characterization started February 2013, test benches at TagusLIP (Lisbon, PT) and INFN (Turin, IT)
- Test results are very preliminary, but very encouraging and match well with simulations
- Next steps: consolidate the electrical tests, assess the performance with a SiPM, coincidence measurements
- If results are confirmed, a further power optimization could reduce the power consumption to less than 4 mW/ch in a future version
Outreach

- **Participation in International Conferences**
  - M D Rolo et al, "TOFPET ASIC for PET applications", 14th International Workshop on Radiation Imaging Detectors, 1-5 July 2012, Figueira da Foz, Portugal
  - M D Rolo et al, "Integrated Circuit Design for Time-of-Flight PET with Silicon Photomultiplier", 8th Workshop on Advanced Silicon Radiation Detectors (3D and p-type), 18-20 February 2013, Trento, Italy

- **Papers in peer-reviewed Journals**
Thank you!
[Stevens89] Andrew E. Stevens, Richard P. Van Berg, Jan Van Der Spiegel and Hugh H. Williams
A Time-to-Voltage Converter and Analog Memory for Colliding Beam Detectors
IEEE JSSC vol 24, no 6, 1989

[Rivetti09] A. Rivetti et al.
Experimental Results from a Pixel Front-End for the NA62 Experiment with on Pixel Constant Fraction Discriminator and 100 ps Time to Digital Converter
NSS MIC Conf. Records 2009
backup slides
Other features of the TOFPET ASIC:

- Data transmission w/ TX training or CLK_out;
- Synchronous/Async. test for the TDC - internal (GCTRL) or external test pulse;
- Monitoring of front-end discriminator output: time, energy, before/after delay line (jitter assessment);
- Usable for p-type or n-type (hole, electron collection) devices;
- Usable with higher light yield crystals (trimmable coarse gain);
- Zin trimming for line impedance adjustment (independent of SiPM DC bias thanks to closed-loop input stage);
- Channel masking for noisy channels;
- Dark-count rate (DCR) and DC+event overlapping measurements;
- Safe-mode power-on
Front-end: single photon count

- Zin trimming for line impedance and BW adjustment is independent of SiPM DC bias thanks to closed-loop input stage.
- FE contribution to total jitter is less than 25 ps FWHM.
- Trigger level can be set down to 0.5 p.e. with SNR above 23 dB ($C_g = 320\,\text{pF} - 9\,\text{mm}^2$ MPPC).
- Phase between trigger and clock edge saved as charge and converted to time domain with a Wilkinson ADC. [Stevens89, Rivetti09]
- 128x time multiplication yields a 50 ps time bin @160 MHz
A low event rate may probably motivate the use of dynamic refresh to the TAC nodes due to the leakage current.
Time and Energy thresholds of 0.5 and 7.0 photoelectrons.

Note 1: \textit{wtac\_T} is a write operation after a time trigger - dark pulses masked.
Note 2: Re-trigger of \textit{DOE\_int} due to scintillation statistics and/or spurious pulses is manageable (\textit{Vout\_E\_AC} is unfiltered)
SiPM+LYSO data - detail of event (*praedictio* mode)

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The energy discriminator input \( V_{out,E,AC} \) can be shaped to avoid re-triggering or to guarantee ToT monotonicity:

Since the shaping is applied as RC filtering, the rise time is degraded - the delay of the DOT signal has probably to be widened: likely to increase jitter
Rejection of dark pulses

- **SYNC**: The latched and synchronous versions of time (DOTL) and energy (DOEL) triggers are polled every clock (acceptance gate up to 1 clk)

- **ASYNC**: A configurable gate (DOE-DOT) generated by analogue circuitry issues external falsehit and validhit flags - spotting of dc+event overlap

- **PRAEDICTIO**: A delayed version of the DOT is masked unless there is an energy trigger
A 6-bit global DAC (current-mode, 20mA conso.) generates a variable amplitude (positive, negative) test pulse, from which an exponential decay is obtained with an RC differentiator.
Time-over-Threshold: internal calibration generator vs. spectre ideal current source

**ToT (Vth, E ~ 7p.e., shaping 5ns) – n-type (BOLD), p-type (DASHED)**

ToT curves for calibration (internal differentiator) and large signal approximate SiPM model. Calibration is with device loading the input: 3x3mm2 SiPM (300pF)

- calibration (e−)
- large signal model (e−)
- large signal model (h+)
- calibration (h+)

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IC Design for TOF-PET with SiPMs

XXVI cycle Seminar
Pre-amplifier, post-amplifier, input Vbl DAC (digital-to-analogue converter), power planes are driven in/out off the chip by dedicated IOs.

Use of triple-well on sensitive/noisy circuits; Digital block (TDC_CTRL + GCTRL) laid in an island isolated by a 20 $\mu$m BFMOAT ring (undoped, highly resistive substrate)

Two regional pad-rings with independent bias and ESD circuitry.
Bias Reference generators, Safe-mode power-on

Internal biasing is configurable by SPI.

- **External bias**: VREF for TDC, 2 golden reference voltages for internal current/voltage bias generators;
- **Each Bias cell** is configurable with a 6-bit DAC;
- **GCTRL** imposes a default configuration vector (tackles SPI problems, noisy power-on, ...) for a testable chip:
  - SiPM Vbl = 650mV
  - Vth_T = 4 p.e.
  - Vth_E = 7 p.e.
  - n-type input
  - nominal 5k TIA gain
  - 'praedictio' mode active
  - TDC - 1 buffer for synchronization (metastability)
  - 5ns shaping of Vout_E
  - ...

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