Development of Integrated Pixel Front-End Electronics in 65nm CMOS Technology for Extreme Rate and Radiation

Luca Pacher

University of Turin
Graduate School in Physics and Astrophysics
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2nd year seminar

Supervisor: A. Rivetti
PhD Tutor: M. Costa

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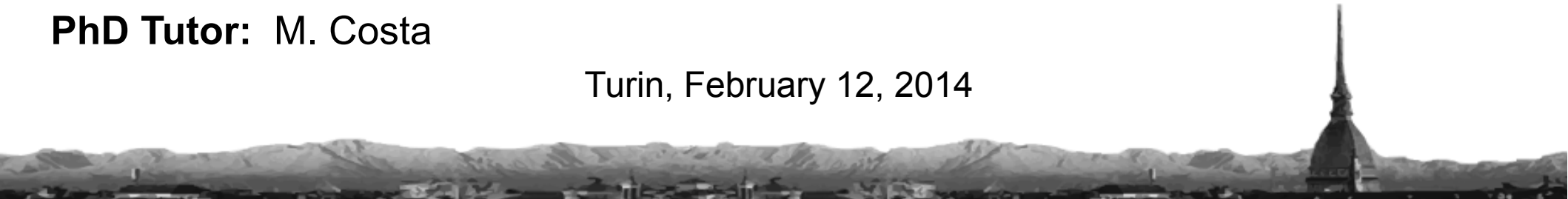
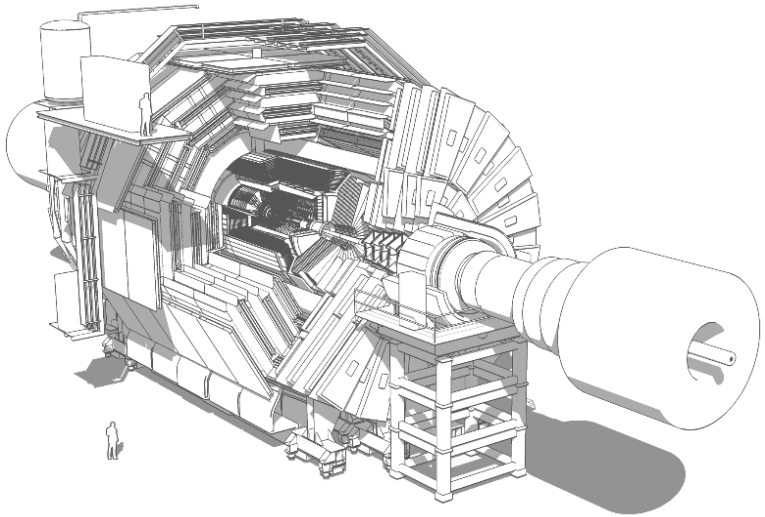


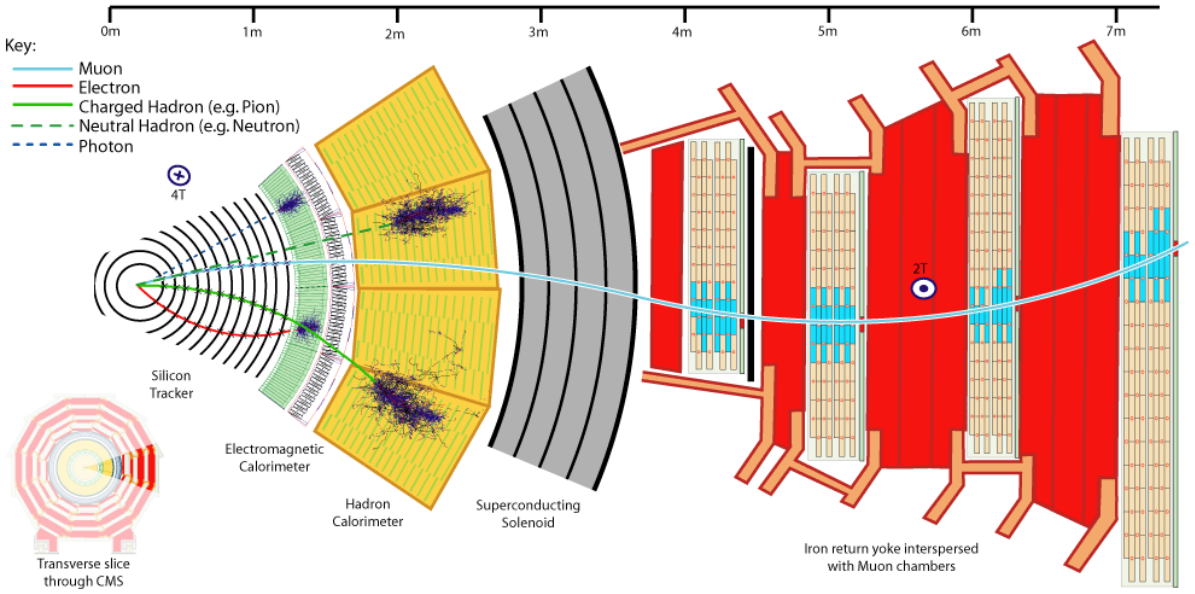
Outline

- Background, framework and motivations
- PhD research activity summary and status report
- Future work and outlook

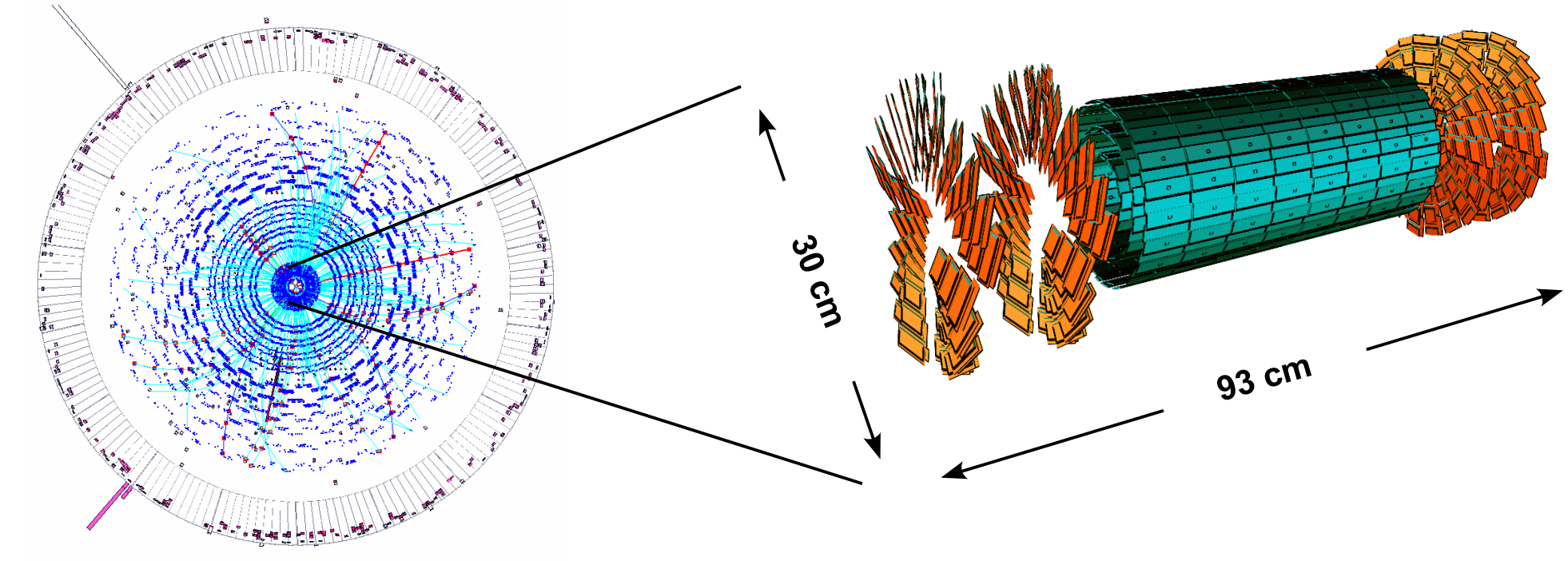
Part I – Background, framework and motivations

The CMS experiment at LHC





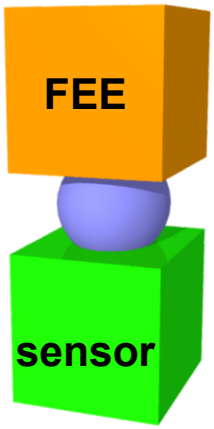
Silicon Pixel Tracker

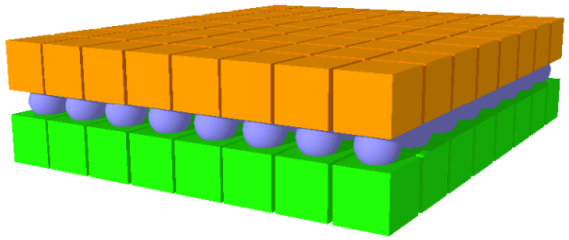


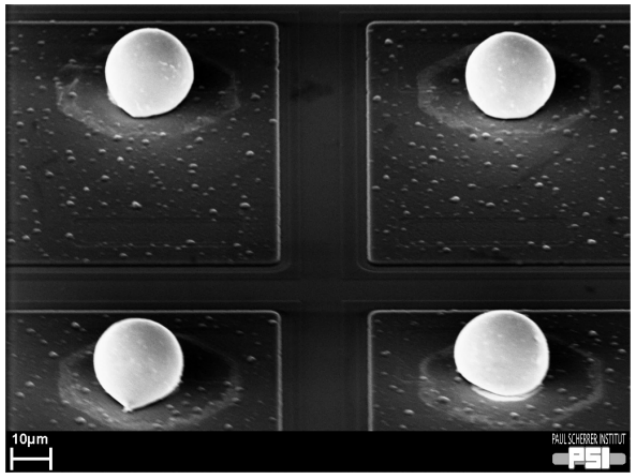
Current CMS silicon pixel detector layout:

- 3 barrel layers (BPIX) + 2 forward disks each side (FPIX)
- coverage $|\eta| < 2.5$, ~ 1 m^2, 66 Mpixels
- track seeding, IP resolution, SV reconstruction
- **hybrid pixel detectors**

CMS hybrid pixel detectors





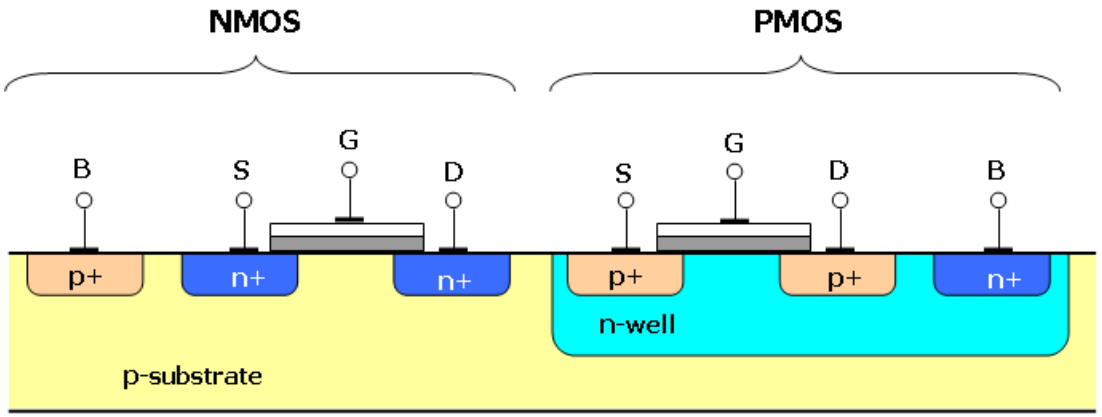


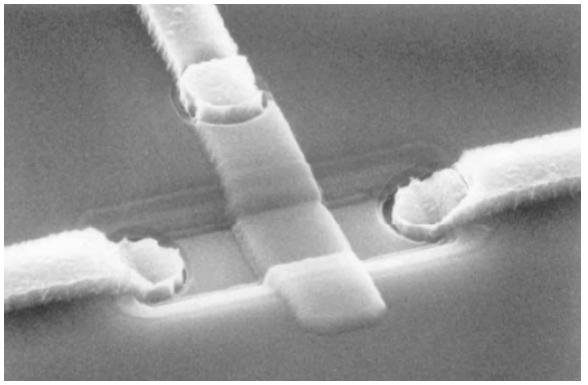
- n^+- on-n **planar** silicon sensors
- 100µm x 150µm **pixel size**
- 280µm **thickness**
- 300V nominal **reverse bias**
- charge collection **by drift** (speed and radiation hardness)
- the charge signal of each pixel is read out by its own dedicated **Front-End Electronics (FEE)**
- **bump-bonding** technique (flip-chip technology)

The readout of a **pixel matrix** requires the design of a high specialized full-custom Application-Specific Integrated Circuit (ASIC) implemented in Very Large Scale Integration (VLSI) **CMOS technologies**

CMOS technologies

technology node = minimum channel length

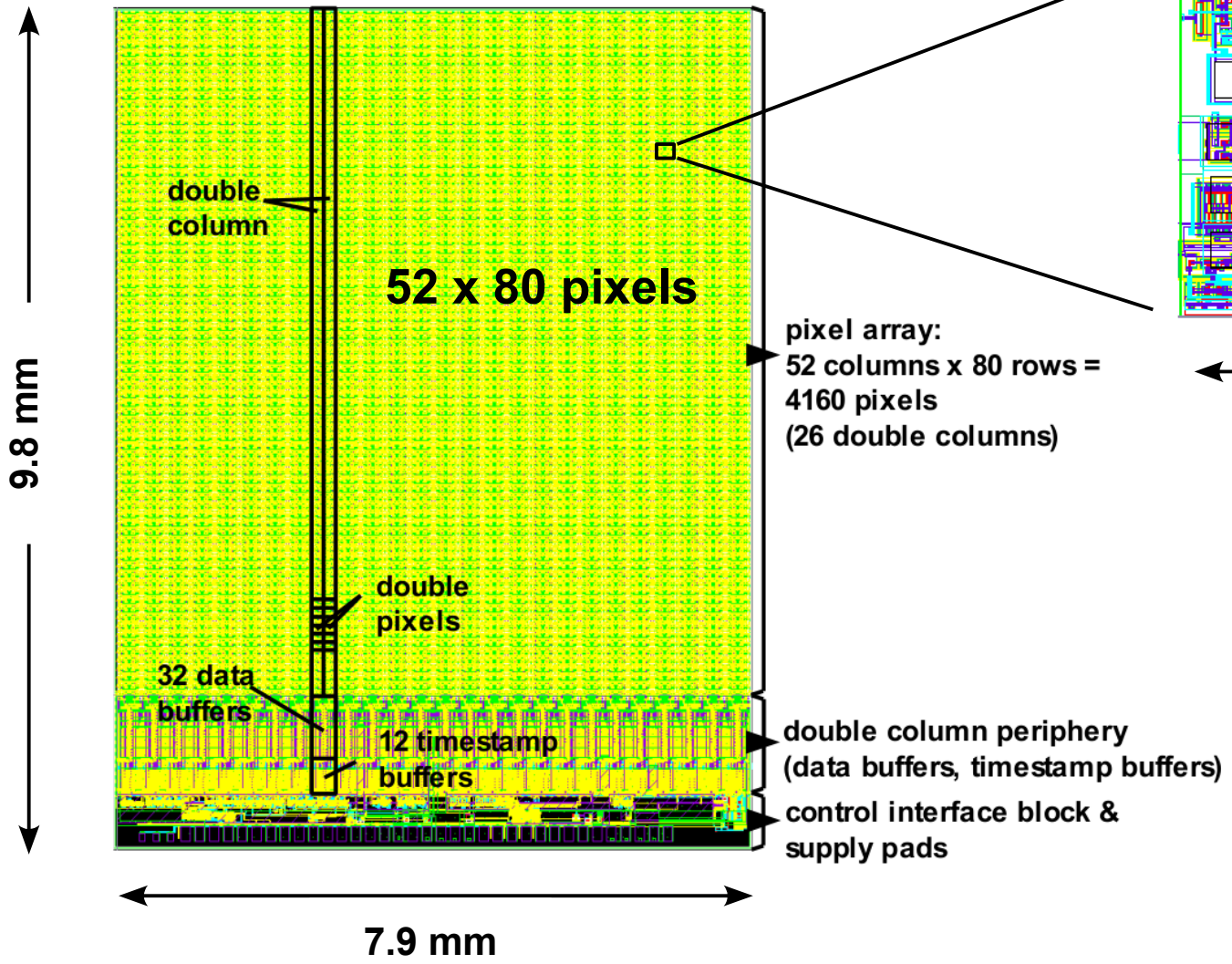




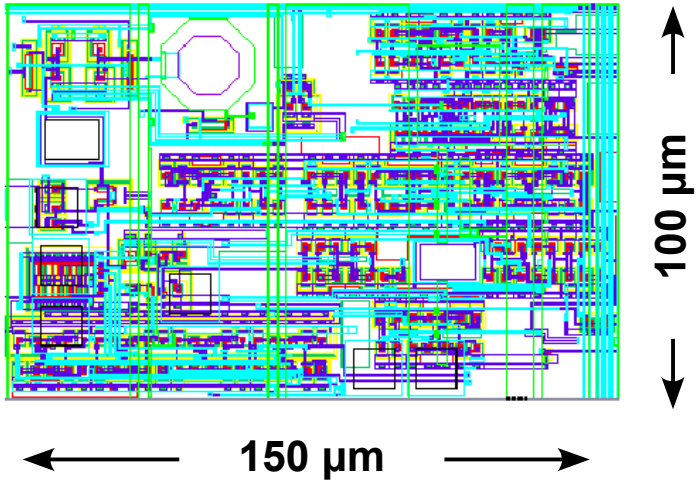
- CMOS fabrication processes dominate the market of **Integrated Circuits (ICs)**
- the **integration density** doubles roughly every 2 years (Moore's Law)
- CMOS technologies represent **the standard solution** for implementing radiation-hard Front-End electronics for particle physics applications in harsh radiation-sensitive environments

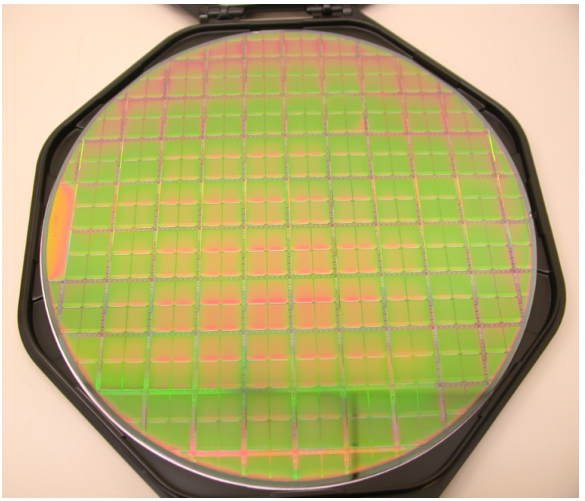
CMS pixel Read-Out Chip (ROC)

0.25 µm 5M CMOS technology (PSI46v2)

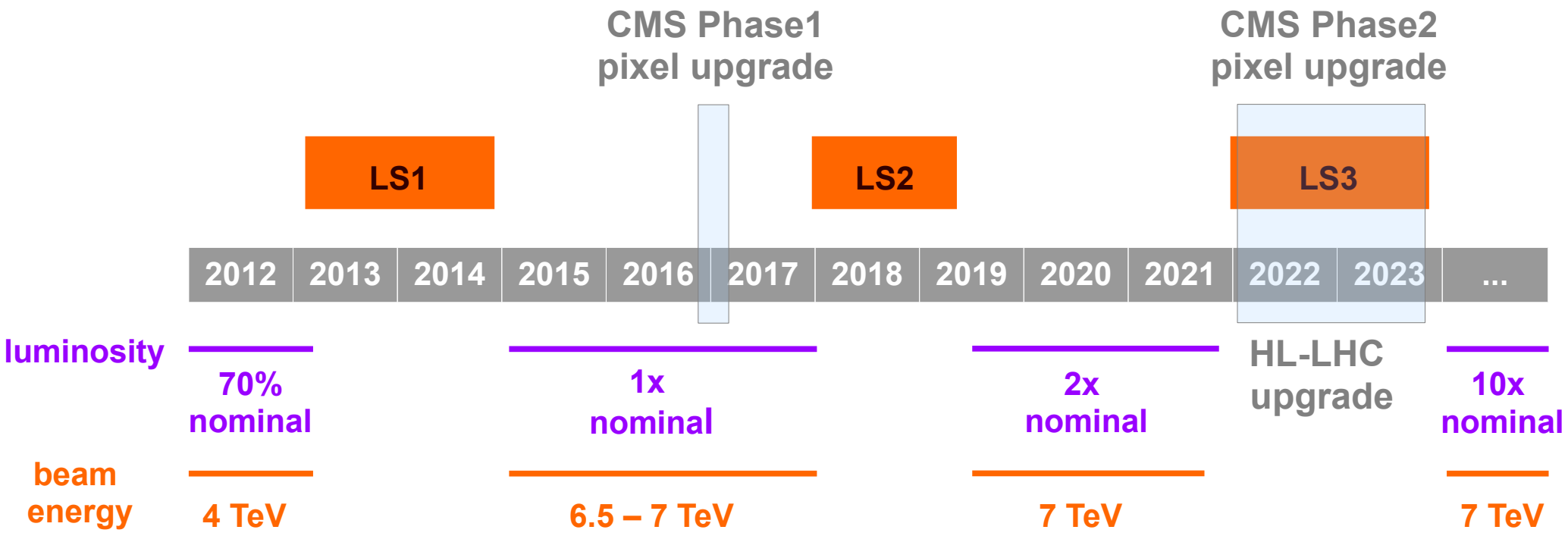


Pixel Unit Cell (PUC)





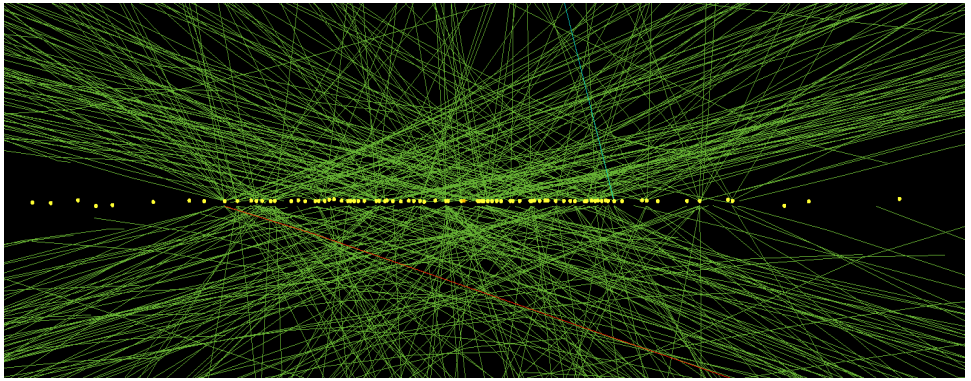
LHC timeline



- 3 main LHC commissioning periods referred to as **Phase0** (up to LS1), **Phase1** (after LS1) and **Phase2** (after LS3)
- **shutdown** time-slots for maintenance and machine performance improvements
  - nominal LHC: 10^{34} cm^{-2} s^{-1} luminosity, 23 fb^{-1}/year in 2012
  - **High-Luminosity (HL) LHC**: 10^{35} cm^{-2} s^{-1} luminosity, 300fb^{-1}/year, foreseen 3000 fb^{-1} in 10 years

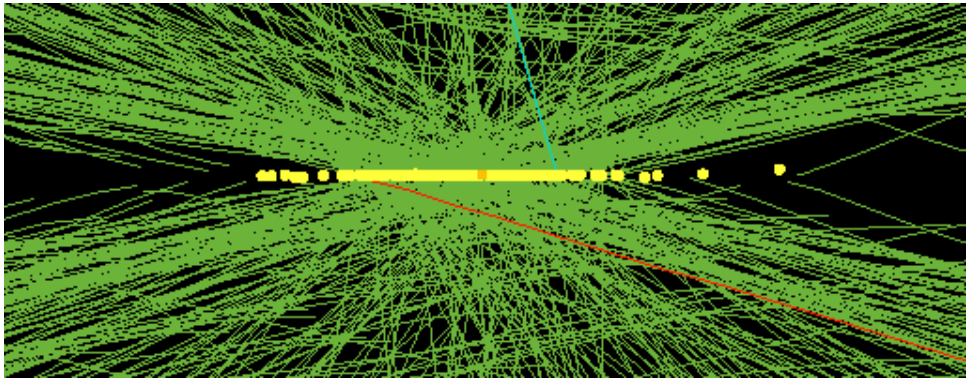
LHC luminosity upgrades

LHC Phase 1



- 2×10^{34} cm^{-2} s^{-1}
- 7 TeV/beam *p-p*
- PU 50-70
- 50-25ns BX

LHC Phase 2



- 10^{35} cm^{-2} s^{-1}
- 7 TeV/beam *p-p*
- PU 140-200
- 25ns BX mandatory

The foreseen HL-LHC upgrade will introduce **unprecedented operating conditions** in terms of **track densities** (10x Phase0) and **radiation levels** (10x Phase0).

CMS Phase 2 pixel upgrade motivations

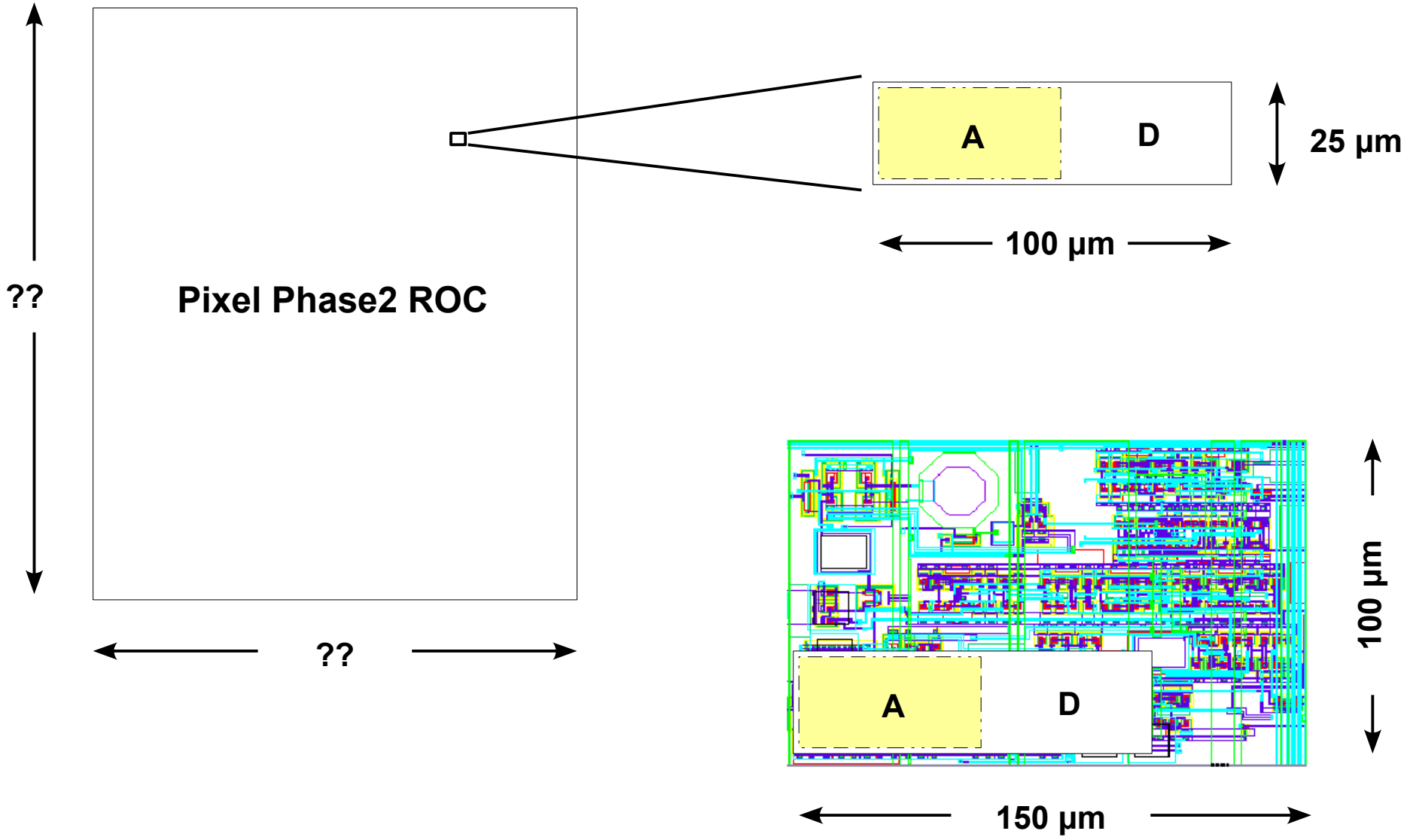
Parameter	LHC Phase0	LHC Phase1	LHC Phase2
luminosity	10^{34} cm^{-2} s^{-1}	$2x10^{34}$ cm^{-2} s^{-1}	10^{35} cm^{-2} s^{-1}
PU	~20	~50	140 or higher
particle flux	50 MHz/cm^2	200 MHz/cm^2	500 MHz/cm^2
pixel flux	200 MHz/cm^2	600 MHz/cm^2	1-2 GHz/cm^2
TID (10 years)	1.5 MGy	3.5 MGy	10 MGy
signal threshold	2.5-3 ke	1.5-2 ke	1 ke or below
L1 trigger latency	2-3 µs	4-6 µs	6-20 µs

The current PSI46v2 chip was designed about 10 years ago to work properly up to $2x10^{34}$ cm^{-2} s^{-1} luminosity and for 100µm x 150µm pixels.

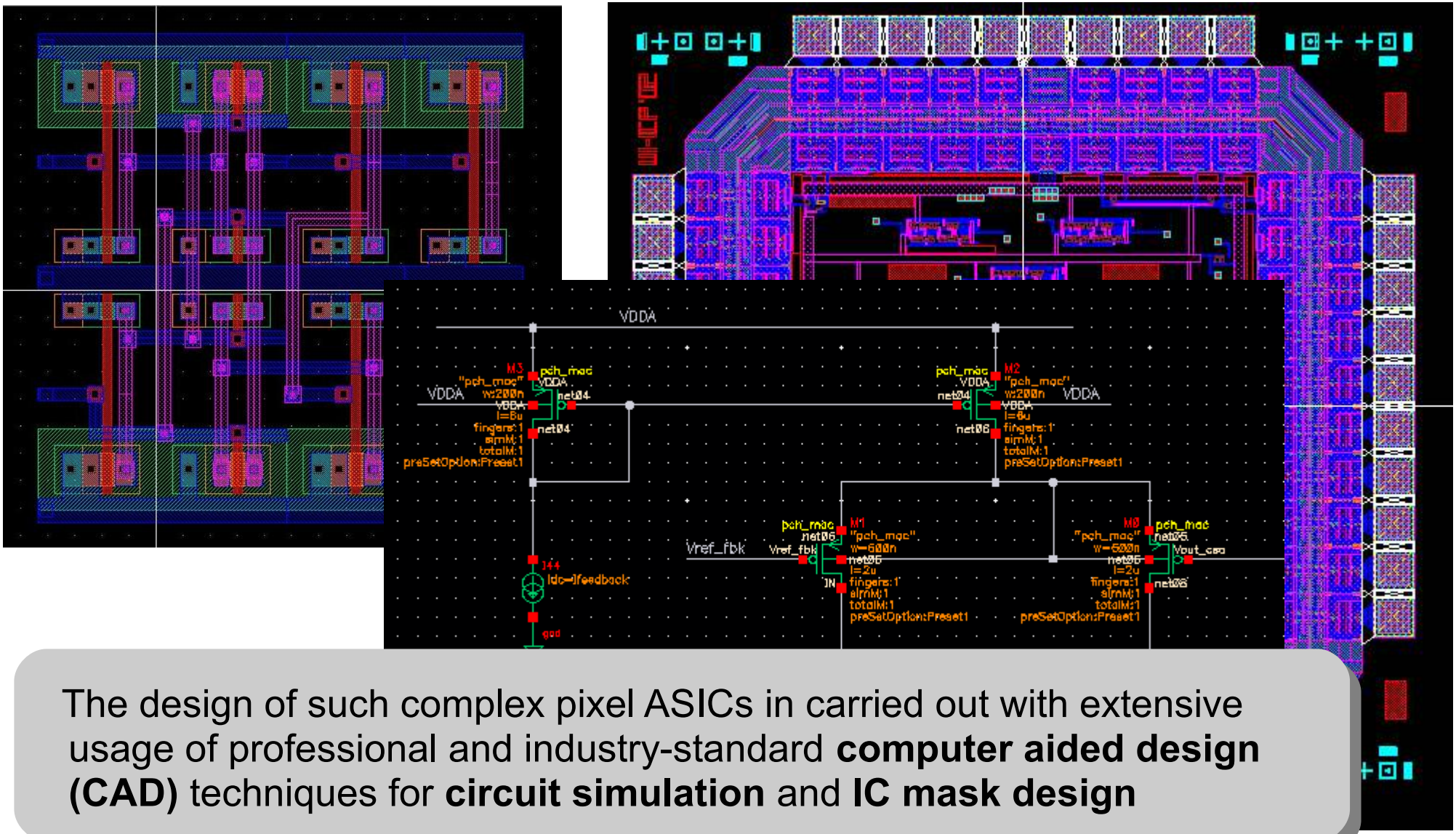
design of a new pixel readout chip required for HL-LHC !

Part II – PhD research work summary

PhD research topic



CAD tools

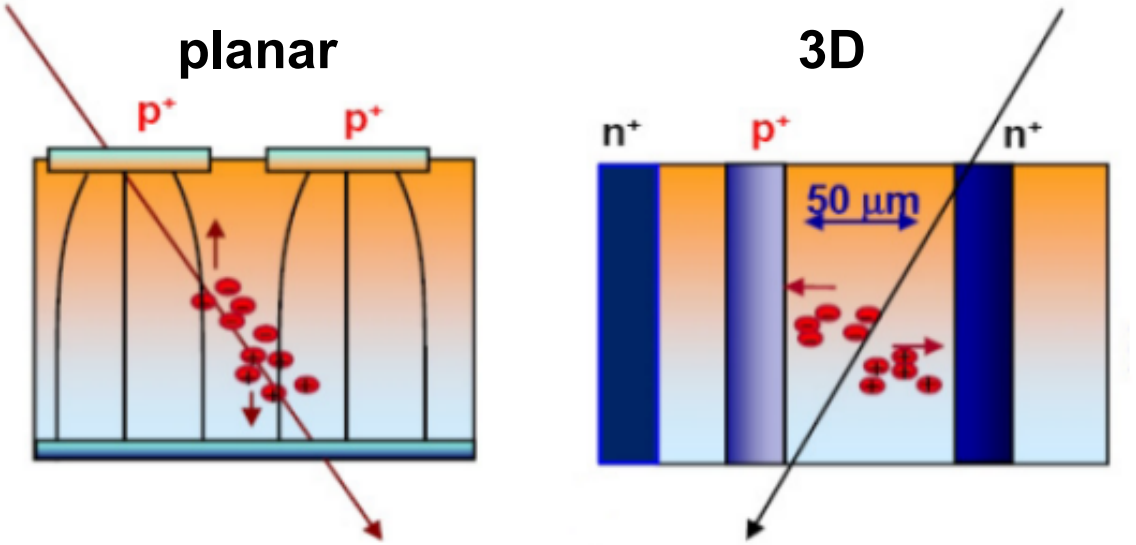


The design of such complex pixel ASICs in carried out with extensive usage of professional and industry-standard **computer aided design (CAD)** techniques for **circuit simulation** and **IC mask design**

New pixel ASIC requirements /1

- sensor choice not yet finalized :
  - very likely planar sensors in the outer layers
  - ongoing RD studies for innermost layers (thin planar sensors? 3D sensors? diamonds?)
  - **sensor-independent** Front-End electronics

- certainly thinner planar silicon sensors to ensure adequate radiation tolerance
  - assume about 100µm thickness (1MIP ~10ke) for Phase2 (280µm current)
  - **low-noise** and **very low-threshold** Front-End electronics requirements



- **50 fF** up to **300 fF** total input capacitance
- **1'000e** minimum detectable charge

New pixel ASIC requirements /2

- increased track densitites
  - **smaller pixel size** for adequate **granularity**
  - assume 50µm x 100µm or 25µm x 100µm (100µm x 150µm current pixels)

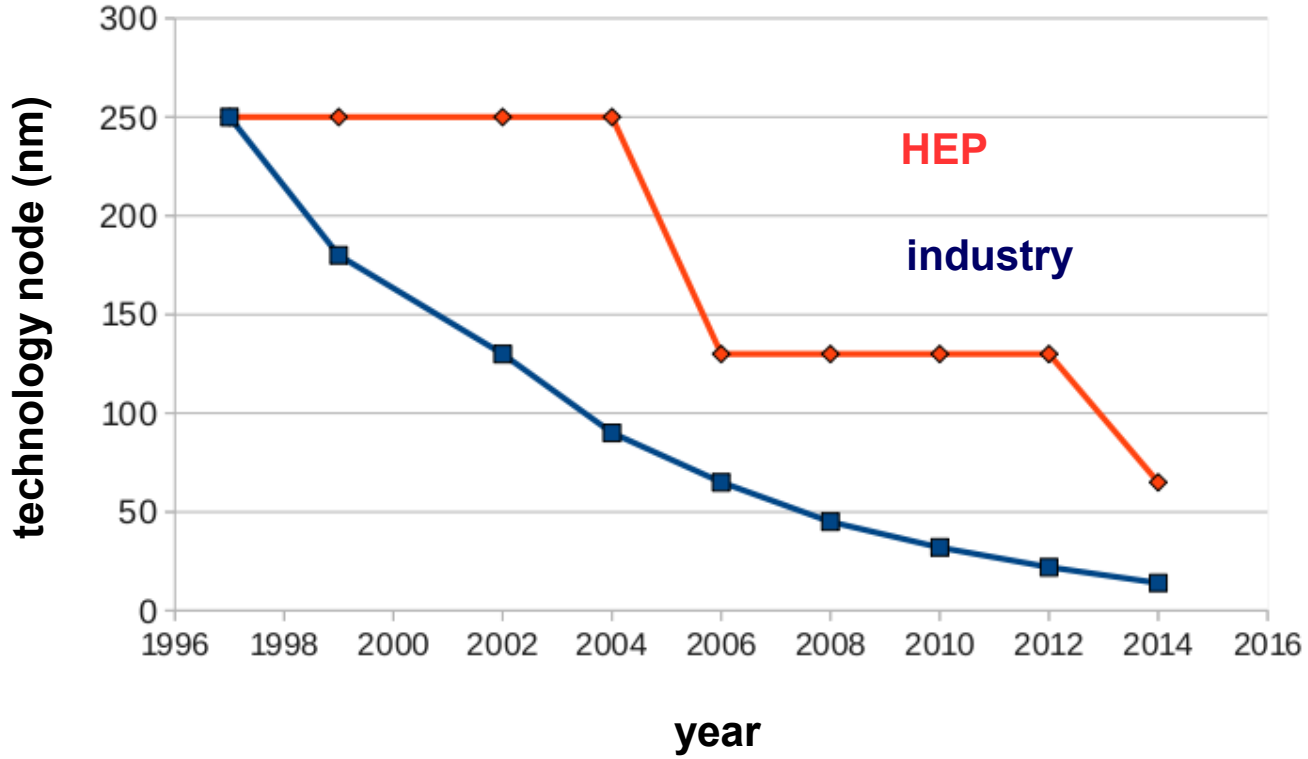
- increased **pixel rates** (assume 2GHz/cm^2 particle flux)
  - 100kHz/pixel with 50µm x 100µm pixels or
  - 50kHz/pixel with 25µm x 100µm pixels

- larger amount of data
  - more **on-pixel intelligence** and local data storage capabilities
  - on-pixel trigger matching for **zero suppression**
  - possible contributions to the L1 trigger?

- **100kHz/pixel** hit rate
- **25µm x 50µm** analog area
- **~6µW/channel** analog power budget

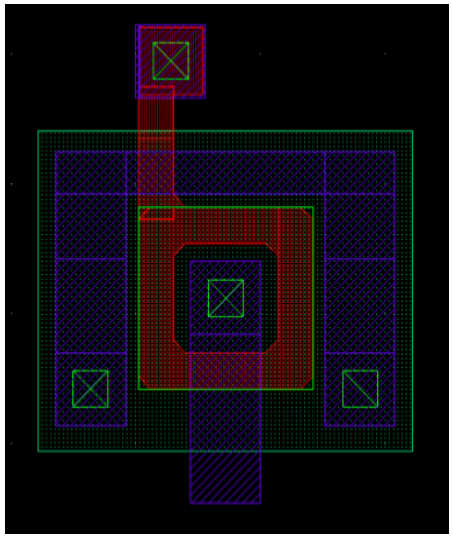
IC technology choice

- a commercial **65nm CMOS** has been chosen by the HEP **pixel community** as the present favored fabrication technology for the Phase2 generation of pixel ASICs
  - present LHC experiments based on a commercial **CMOS 250nm**
  - Phase1 LHC experiment upgrades will also exploit **CMOS 130nm** (e.g. FE-I4 chip for the ATLAS IBL, GBT project)

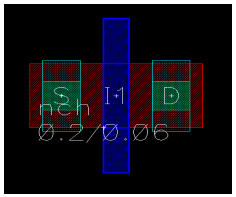


Why 65nm ? /1

- the **radiation tolerance** increases with technology scaling (thinner gate oxides)
- radiation-hardened design techniques with Enclosed Layout Transistors (ELT) no more required
- 65nm demonstrated to be radiation tolerant up to 2 MGy TID, better than 130nm (now to be confirmed up to 10 MGy)



full-custom library
0.25µm ELT nMOS



standard library
65nm nMOS

Why 65nm ? /2

- **low power**
  - 1.2 V supply voltage as 130nm (2.5 V in 0.25µm)

- a 65nm offers **higher integration densities** w.r.t. 130nm
  - chance of implementing more **on-pixel intelligence** for efficient zero suppression schemes (on-pixel trigger matching)

- **improved speed** (~GHz)

- **mature technology**
  - introduced ~10 years ago
  - long term support and availability (OK for Phase2 ~2022)

- at present the 65nm represents **the most advanced technology node** adopted to implement full-custom solutions for radiation detection and measurements in particle physics and medical applications

New communities on 65nm /RD53

- similar requirements (and uncertainties) between ATLAS/CMS experiments Phase2 pixel upgrades
  - joint ATLAS/CMS collaboration for sharing efforts in **technology qualification**
  - collaboration extended to other groups interested in designing in 65nm

- new **RD collaboration proposal** for the development of pixel ASICs in 65nm technology presented to the LHCC in June 2013

- project now approved and officially supported by CERN as **RD53**

- ~ 20 institutes from around the world
  - about 100 collaborators, 50% ASIC designers
  - **strong Italian component** from INFN institutes (Bari, Bergamo/Pavia, Padova, Perugia, Pisa and Torino)

New communities on 65nm /CHIPIX65

- **Italian** CMS/ATLAS groups submitted in July 2013 a detailed proposal to INFN CSN5 to finance a new RD on CMOS 65nm for the next three years
  - Bari, Milano, Padova, Bergamo/Pavia, Perugia, Pisa and Torino INFN institutes involved
- **CHIPIX65** approved in October 2013
  - 700 kEuro funding, ~2 MPW submissions/year
  - 35 members, 20 ASIC designers
- research activities divided into different **working packages**
  - radiation hardness
  - analog electronics
  - digital electronics
  - chip integration
- **first submission** to the foundry planned for June/July 2014

2012/2013 research activity summary

- **UNIX system administration** and support for CMS 65nm design activities in Turin
  - design kit installation and maintenance
  - CAD tools setup and usage
- **65nm design kit test and characterization**
  - full design-flow test and understanding
  - technology and models characterization
  - documentation

65nm completely new in Turin !

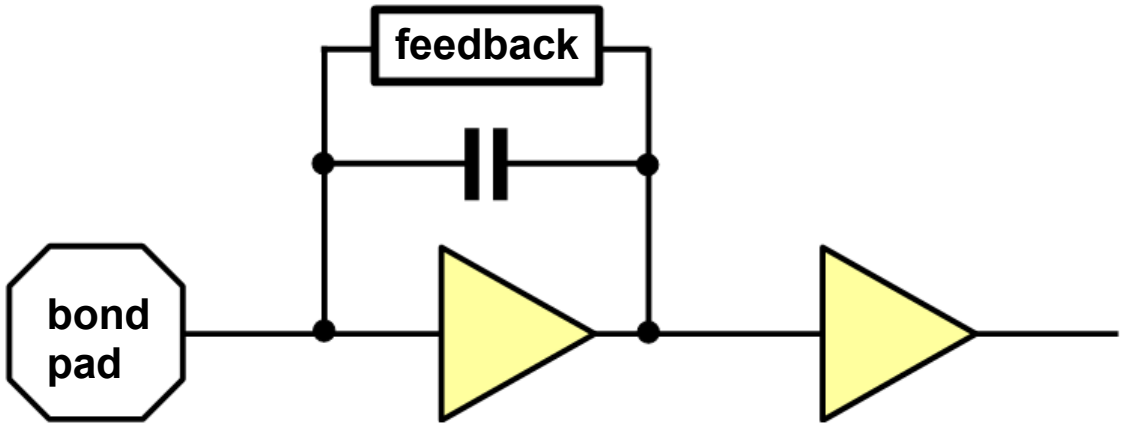
- **design and simulation** of different analog and mixed-signal blocks
  - high open-loop gain inverting amplifier for charge sensitive amplifier (CSA)
  - track-and-latch comparator with autozeroing
  - basic library of custom digital gates
  - auxiliary digital control logic
  - 5-bit SAR ADC with asynchronous control logic

IC design in 65nm

- digital design gains from **technology scaling** in terms of speed, integration density (higher functionality) and power/gate

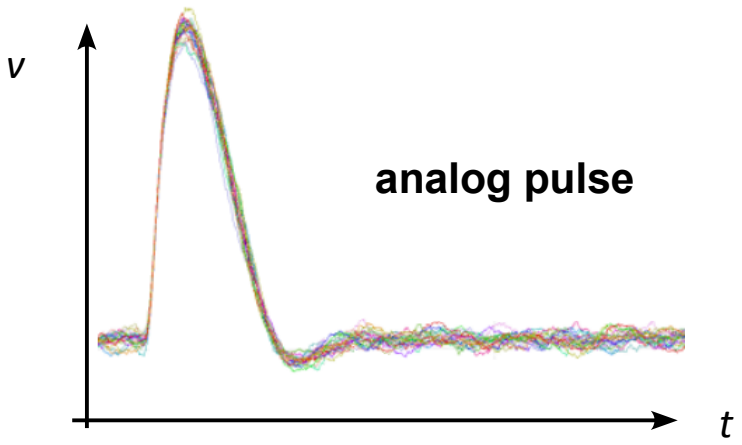
- **analog design more challenging**
  - increased device-modeling complexity and number of **design rules**
  - **short channel effects** cannot be neglected
  - reduced **voltage headrooms** and single-transistor **intrinsic gain**

Pixel Front-End basics /Signal formation



charge-to-voltage conversion (CSA)

signal formation (SHAPER)



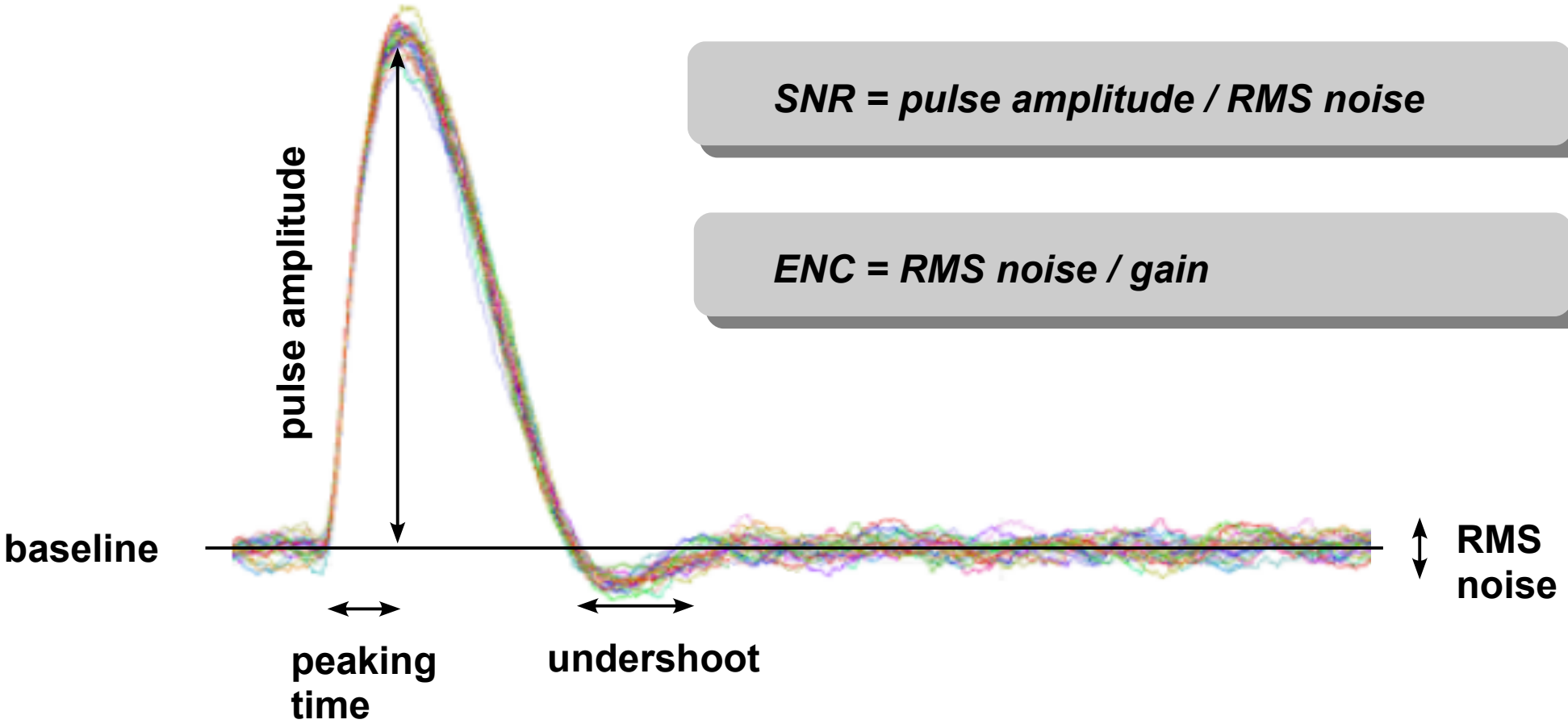
- **charge-to-voltage conversion** provided by a charge-sensitive amplifier (CSA)
- further **signal shaping** and **noise reduction** can be achieved by means of a dedicated filering stage (SHAPER)
- a complex **feedback network** is required to discharge the feedback capacitance and to compensate the sensor **leakage current**

Pixel Front-End basics /Analog pulse

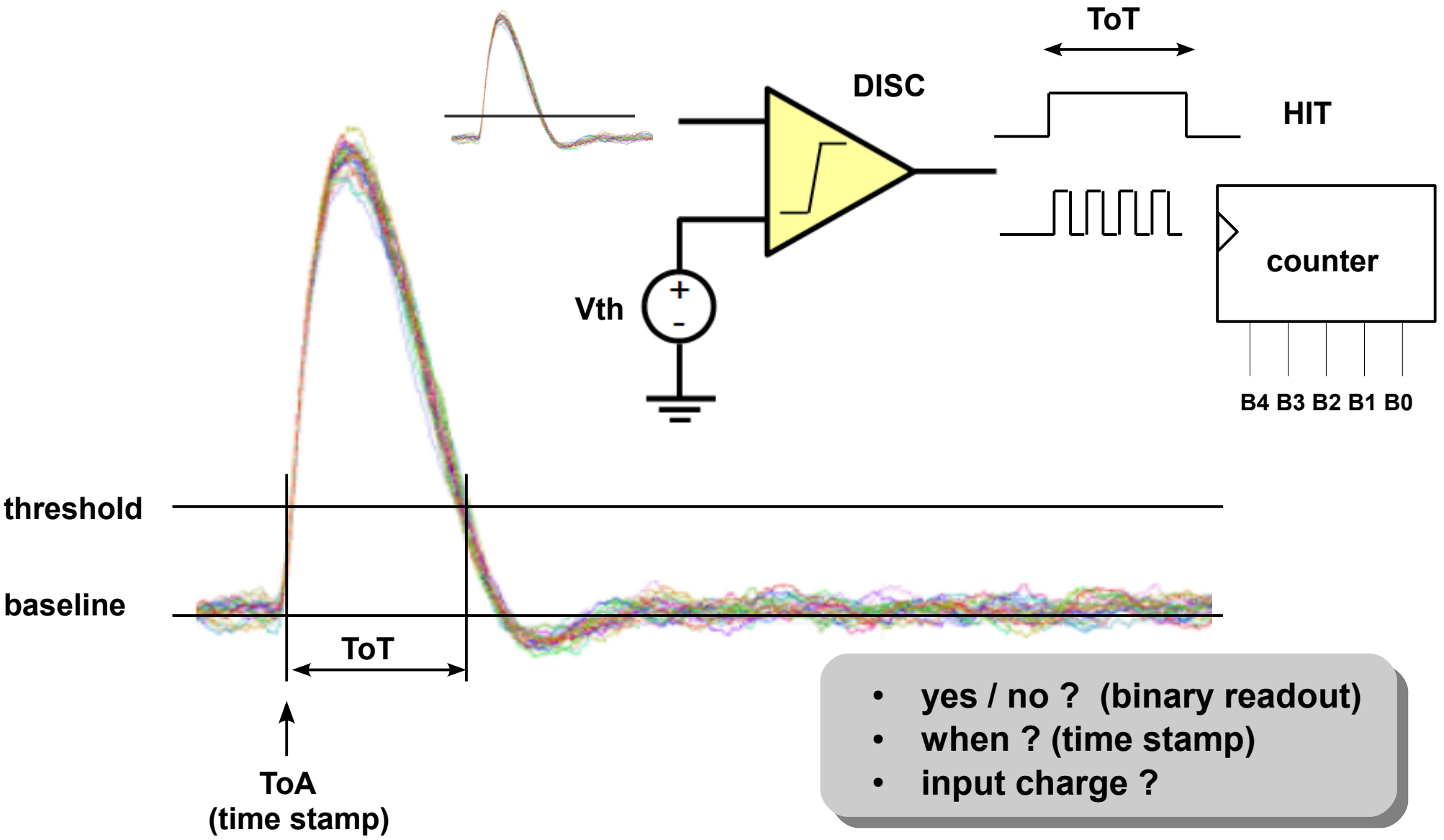
gain = pulse amplitude / input charge

SNR = pulse amplitude / RMS noise

ENC = RMS noise / gain



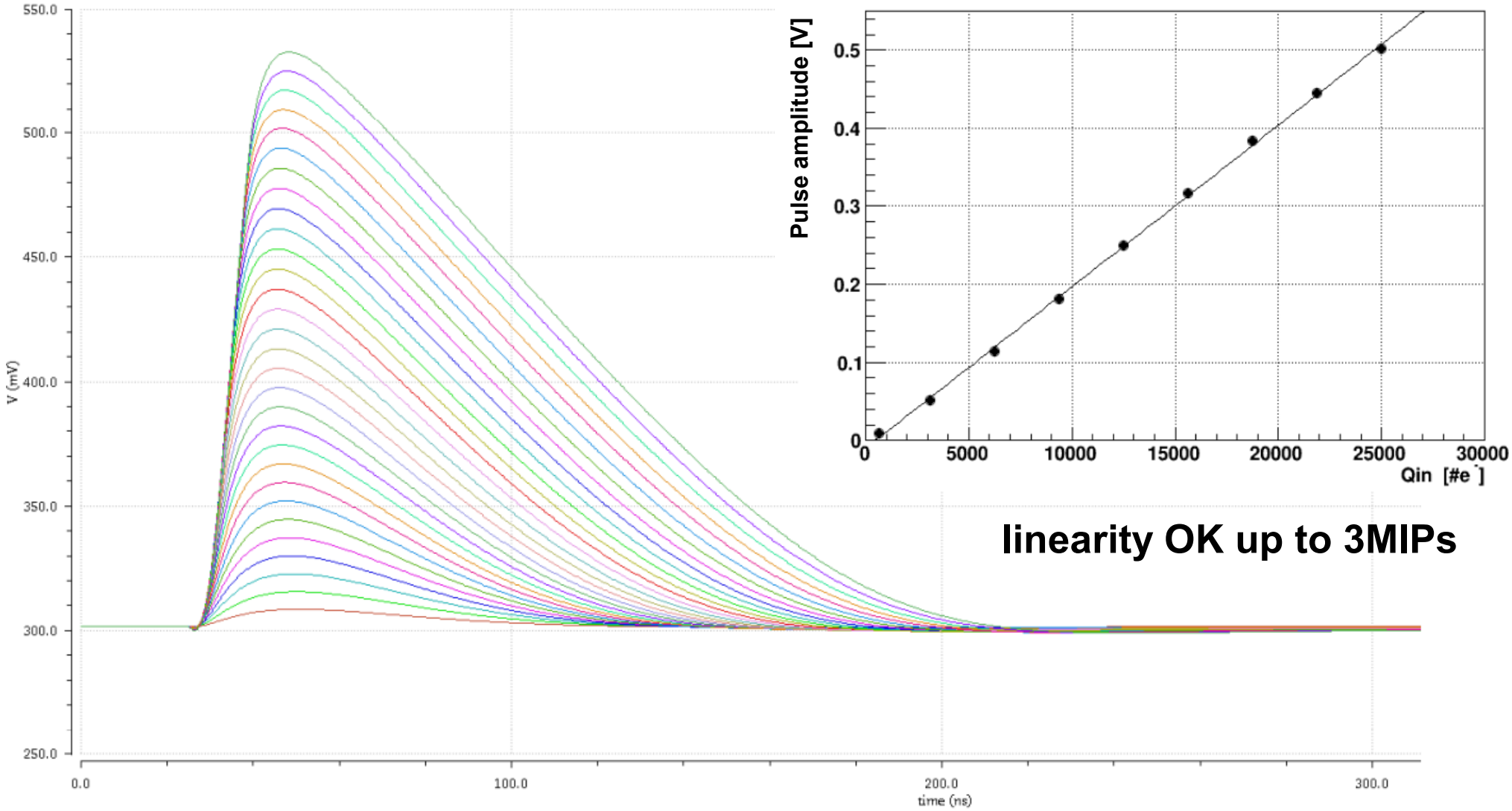
Pixel Front-End basics /Hit discrimination



- yes / no ? (binary readout)
- when ? (time stamp)
- input charge ?

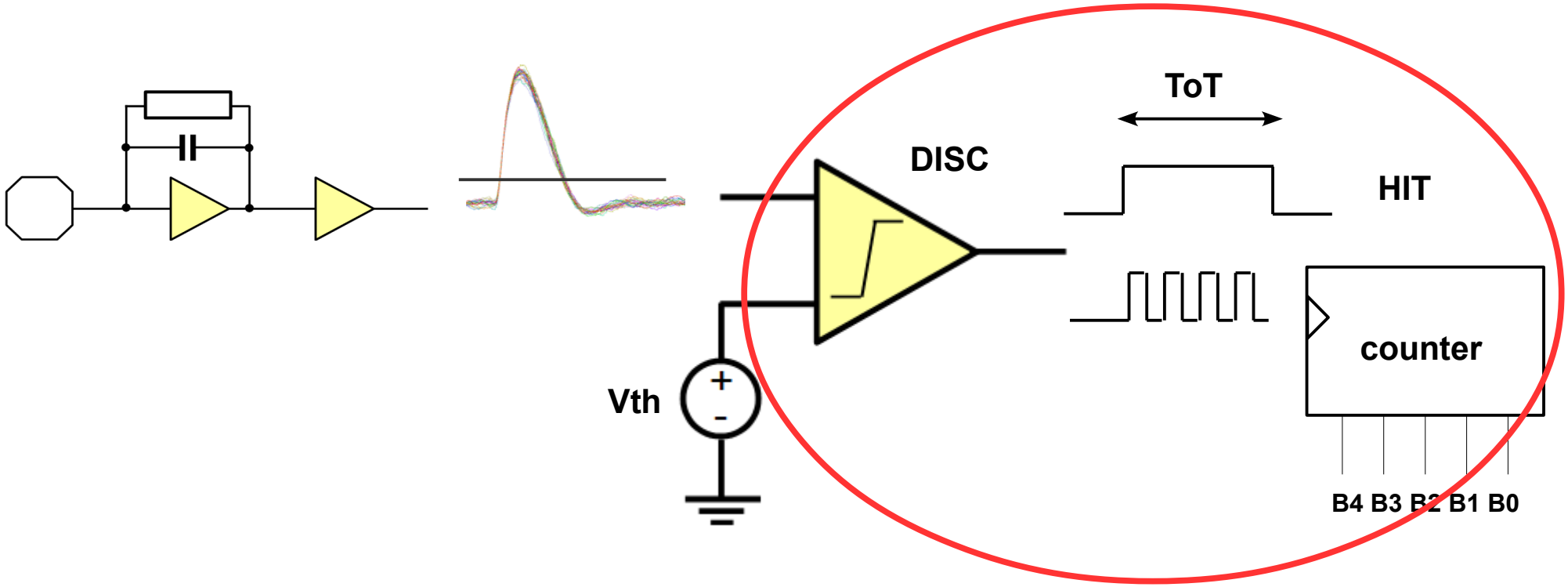
CSA/shaper design

1MIP ~10'000e for 100 µm thickness silicon sensors



linearity OK up to 3MIPs

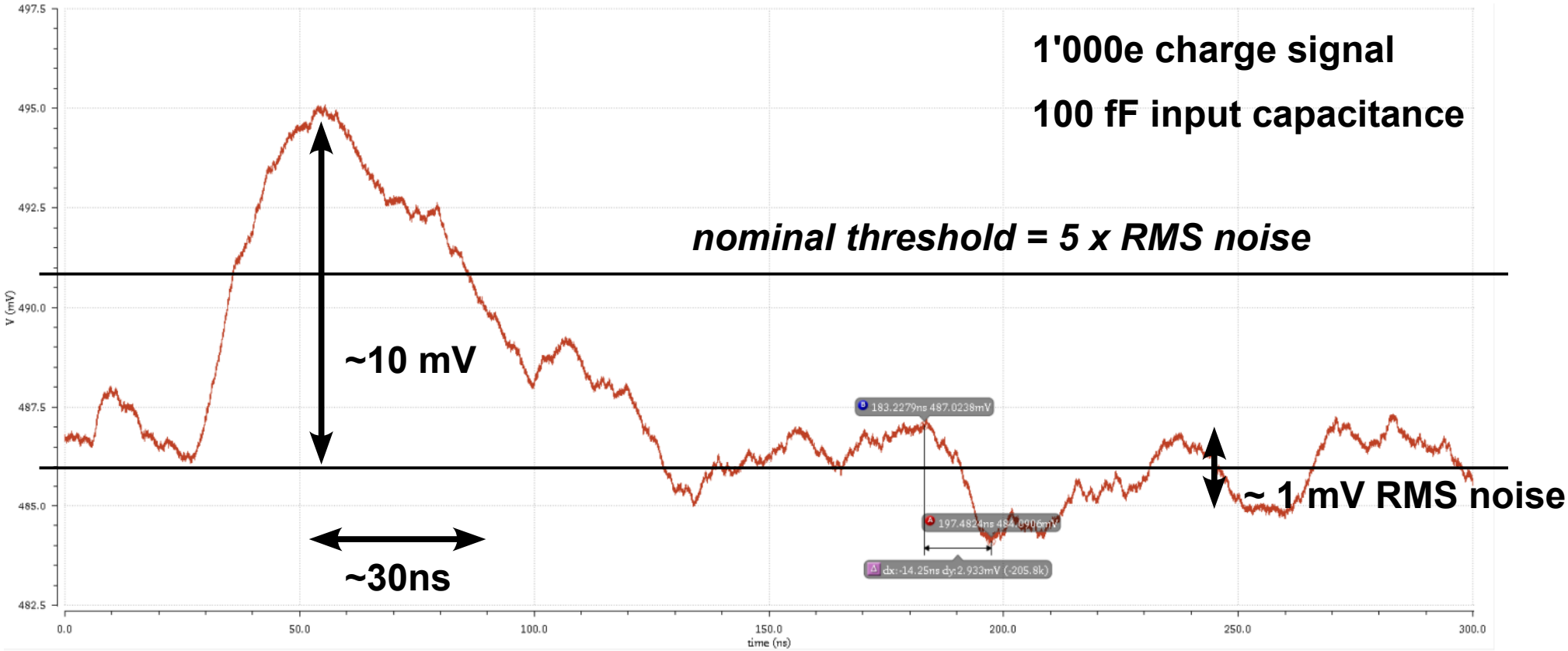
Analog brainstorming



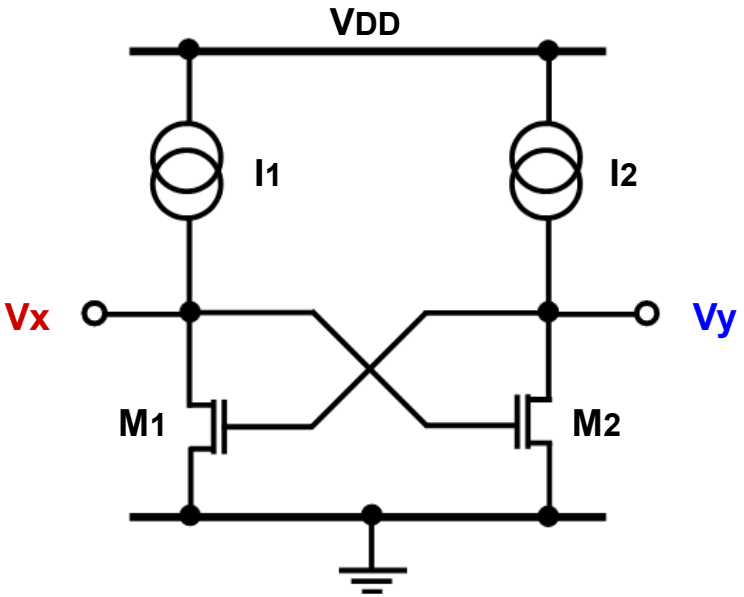
- try to explore **innovative solutions** for hit discrimination and charge encoding
- take advantage of the **speed** offered by a **65nm CMOS**
- what about a ***synchronous*** Front-End approach ?

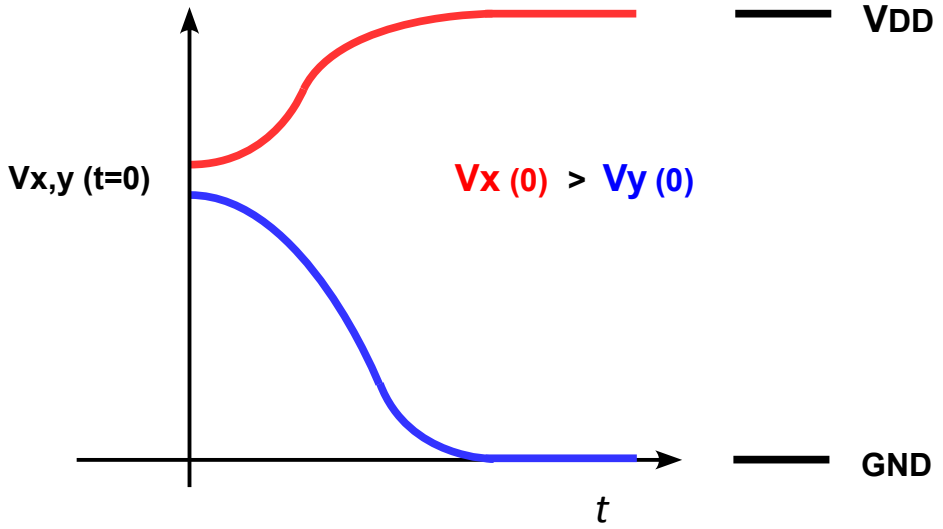
Minimum detectable charge signal

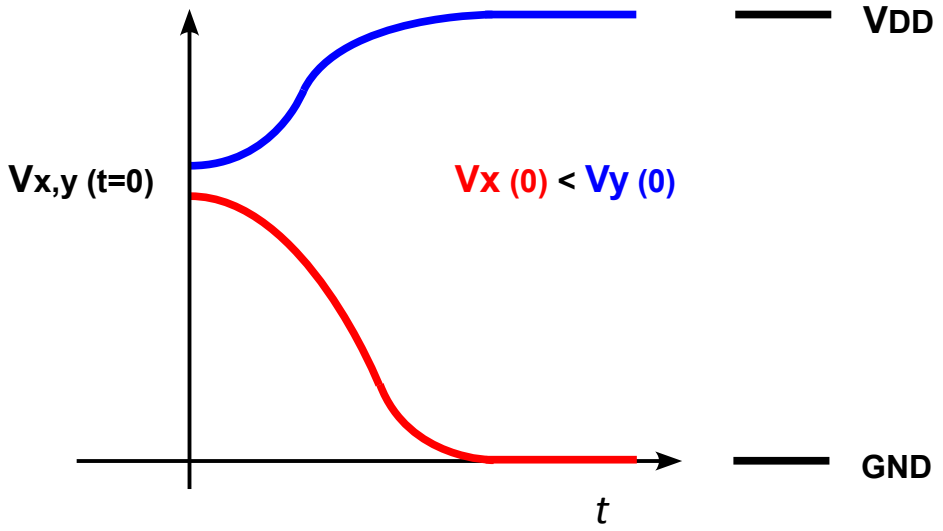
- the challenge is to discriminate pulses of a few mV above the nominal threshold
- requires the design of a **high-speed** (~1ns) and **high-resolution** (~mV) comparator



Positive feedback /1

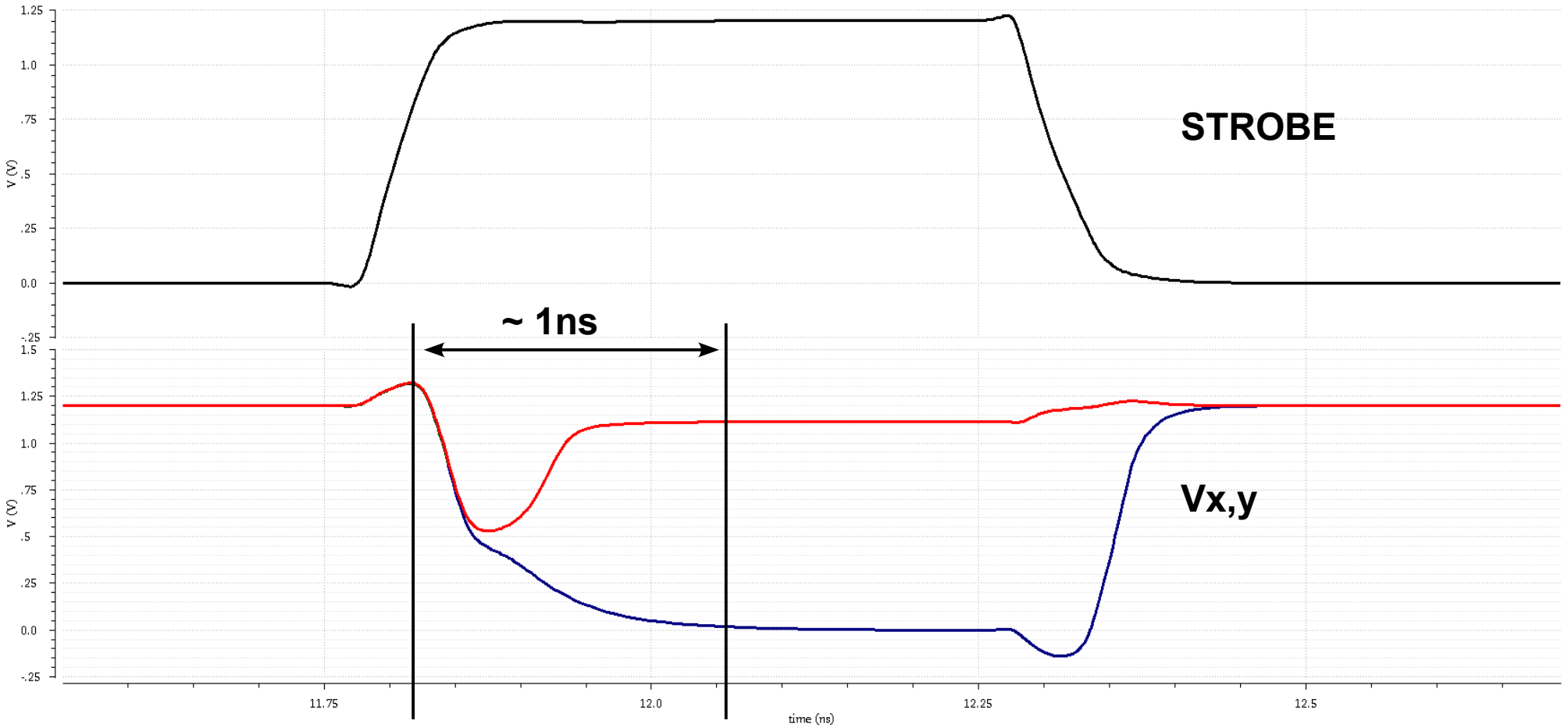




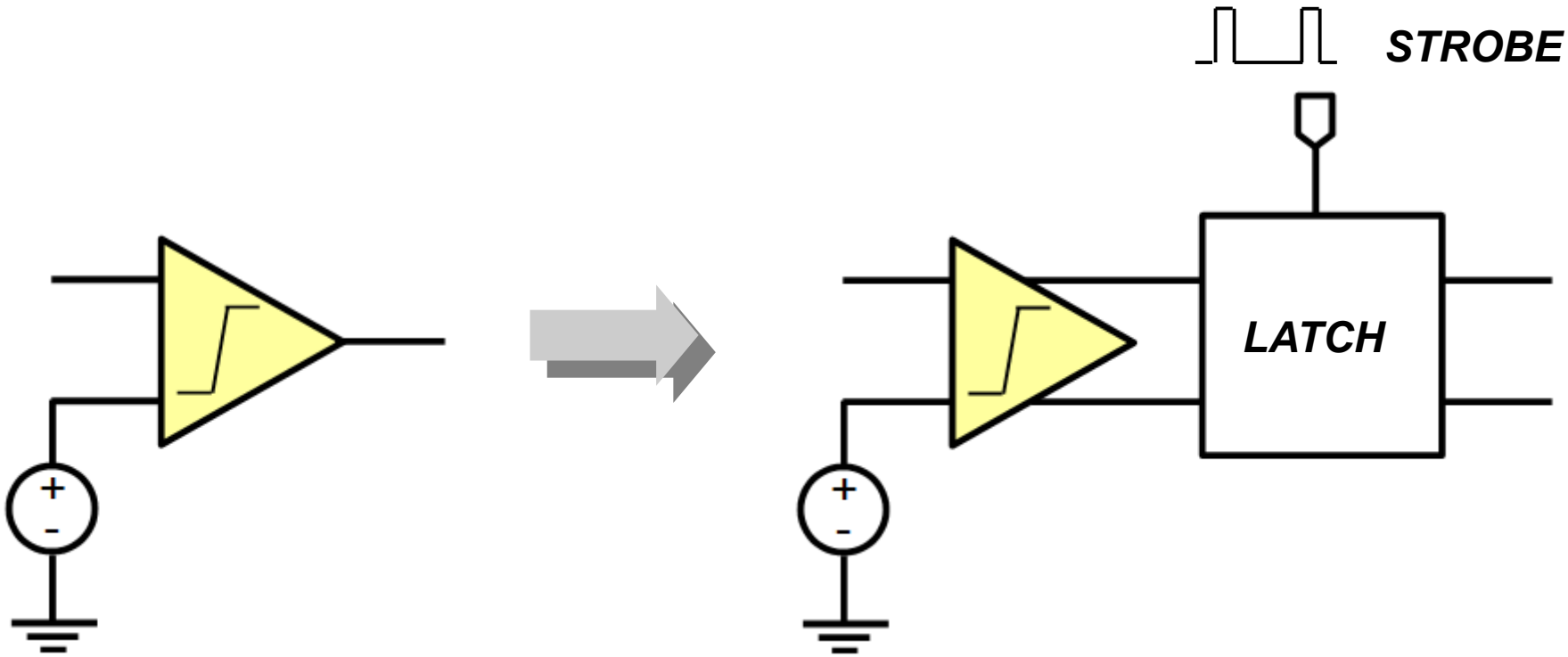


Positive feedback /2

- thanks to the usage of positive feedback the comparator decision is promptly ready within ~ 1ns
- fast signals of a few mV above the nominal threshold can be discriminated



Synchronous Front-End approach /1

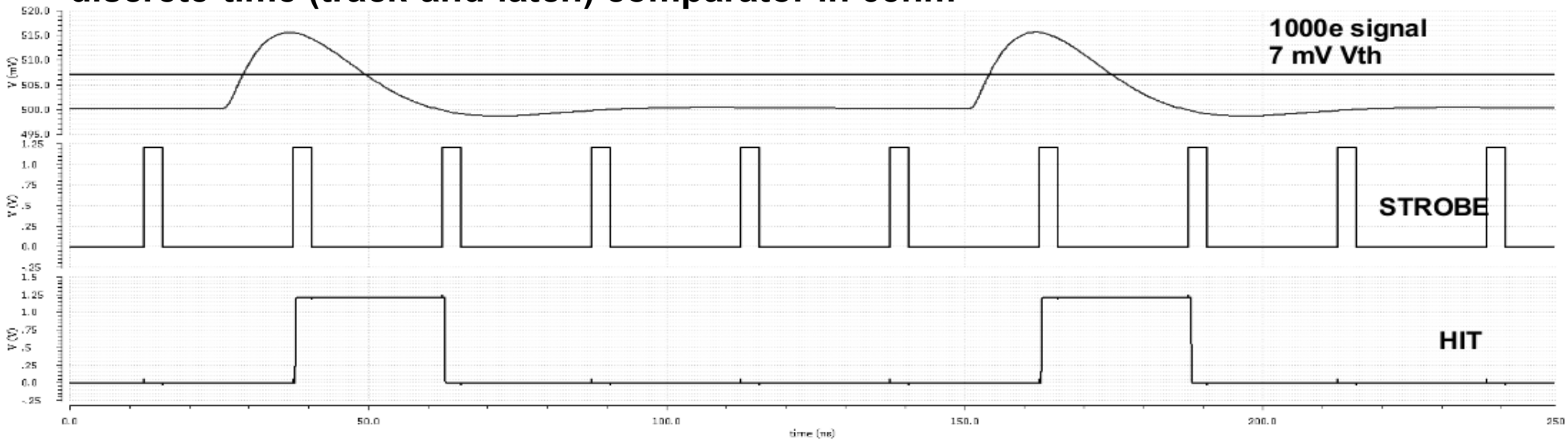


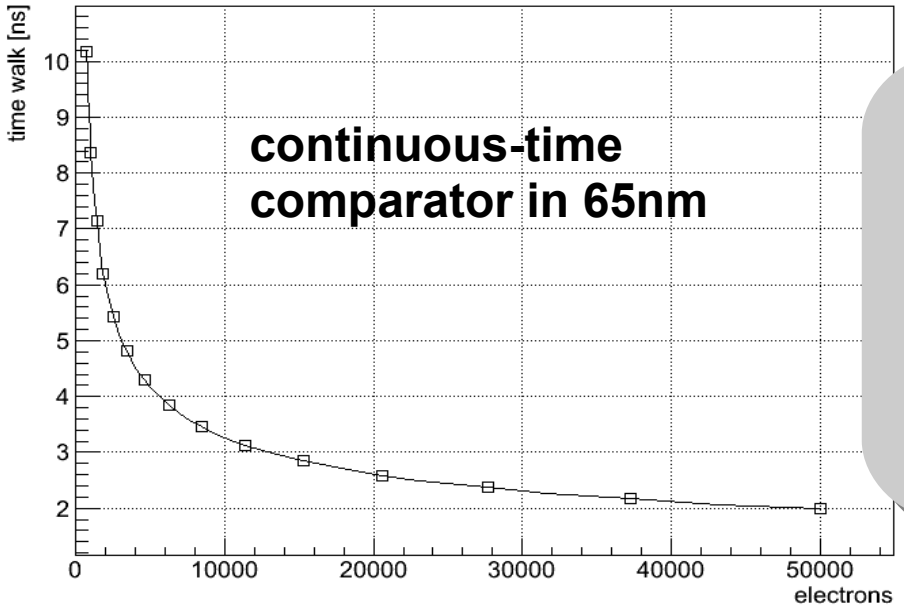
continuous-time comparator

track-and-latch comparator

Synchronous Front-End approach /2

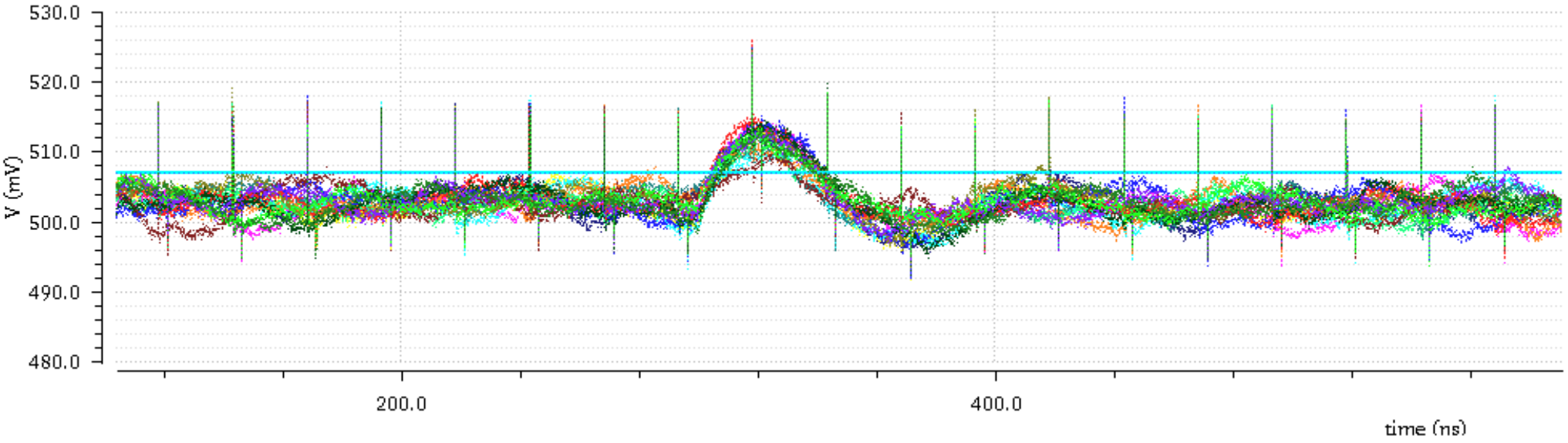
discrete-time (track-and-latch) comparator in 65nm



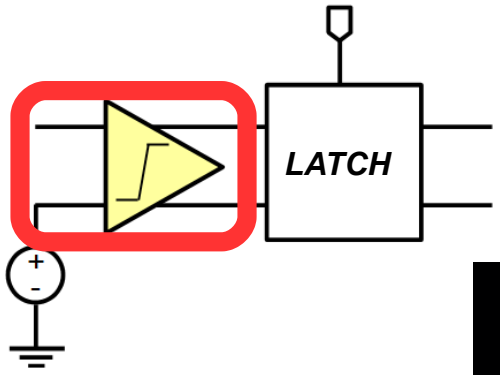


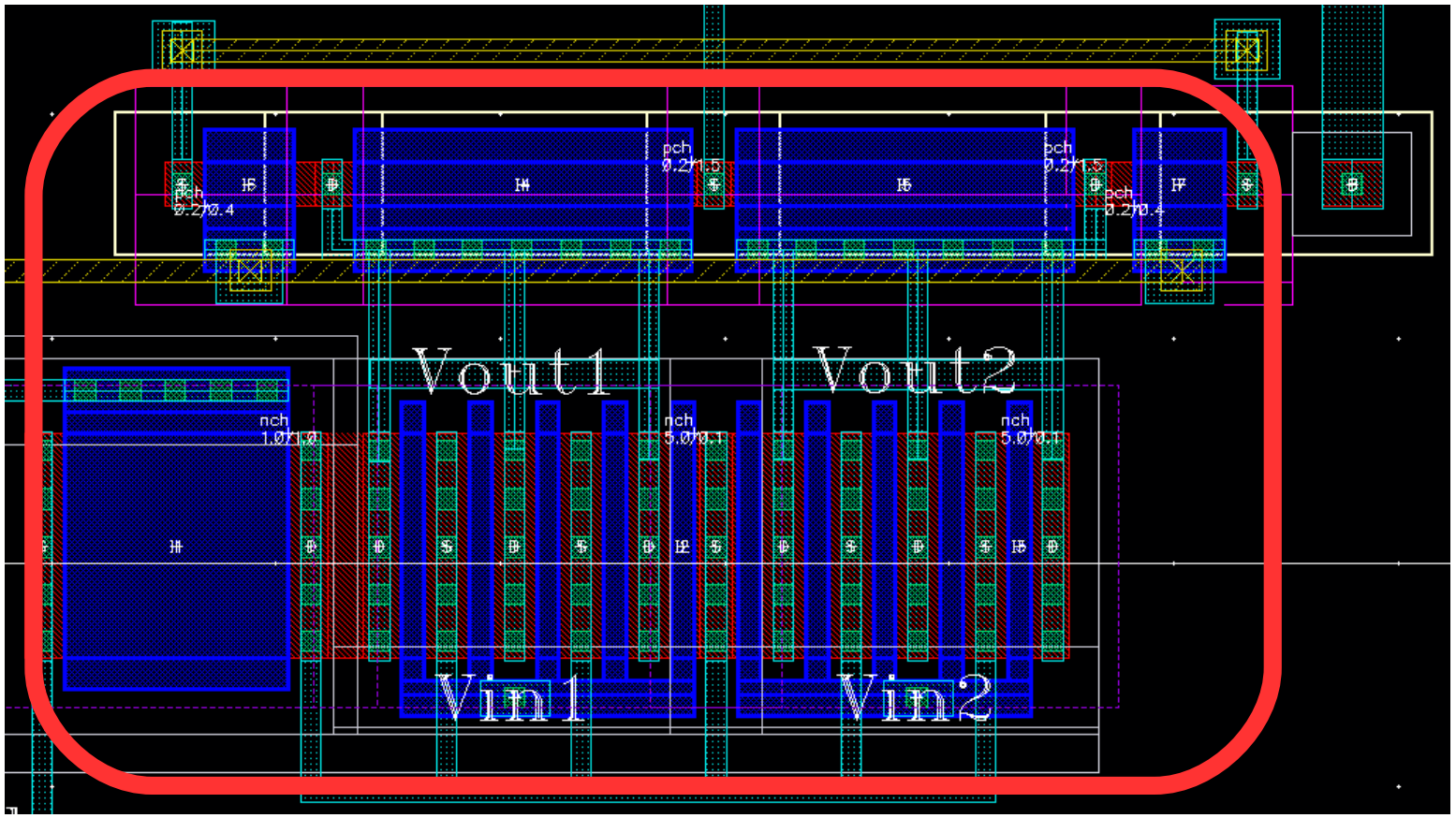
- hit generation **synchronized** with a 25ns bunch crossing (12.5ns peaking time)
- the **delay** becomes an almost constant and well defined quantity ~peaking time
- **no time-walk issues** in the time stamp assignement

Complete analog chain simulation



Layout example





4 µm

8 µm

Conclusions and outlook

Next steps and future work

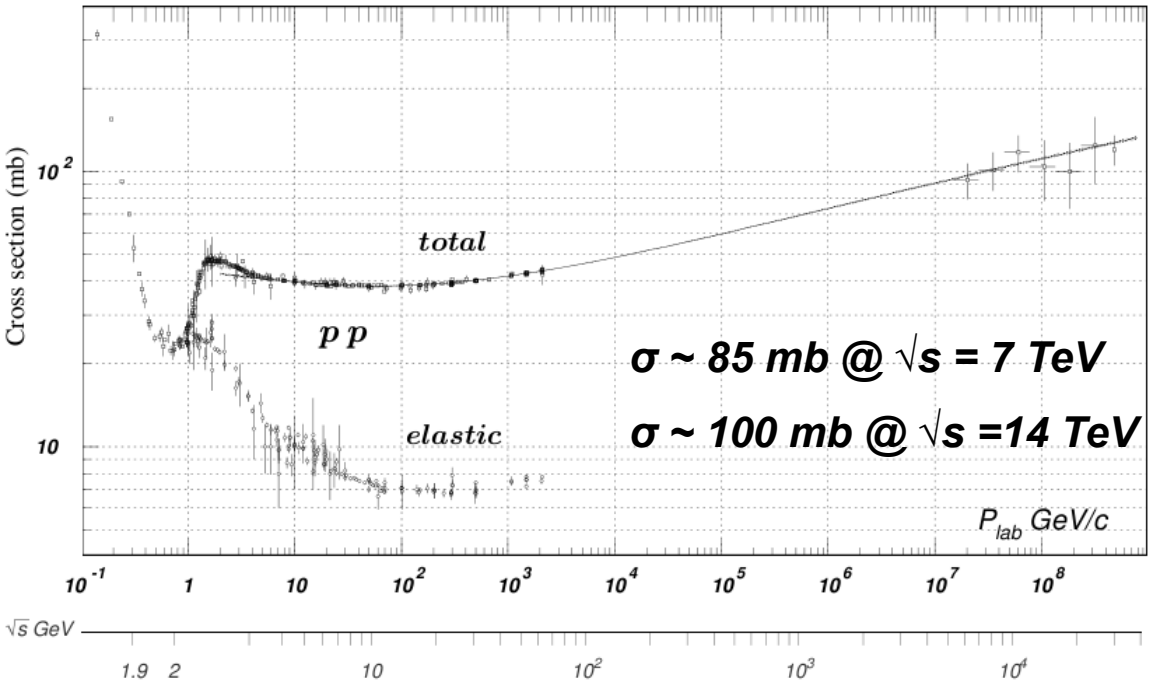
- the **CHIPIX65 collaboration** is planning to submit a 3mm x 4mm Multi Project Wafer (MPW) to the foundry in ~Spring 2014
- design of an innovative charge encoding based on a local **asynchronous digital control logic for ToT measurements**
- on-line calibration with **autozeroing techniques** is under investigation
- finalization of the **complete layout** for the analog part
- **test-bench characterization and measurements** with first prototypes

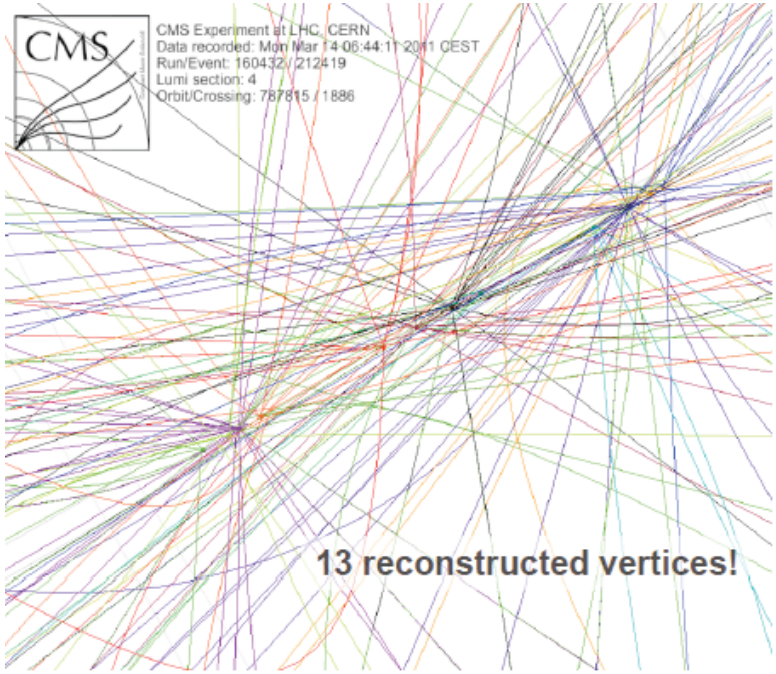
Summary

- HL-LHC operating conditions very challenging (PU, radiation levels)
- my PhD research activity is devoted to the design of innovative solutions for **pixel ASIC analog Front-End electronics** suitable for the foreseen Phase2 CMS pixel upgrade
- a commercial **65nm CMOS** has been chosen by the HEP pixel community as the present favored fabrication technology for the next generation of pixel ASICs
- at present the 65nm represents **the most advanced technology node** adopted to implement full-custom solutions for radiation detection and measurements in particle physics and medical applications
- new 3-years joint ATLAS/CMS collaborations **RD53** and **CHIPIX65** are devoted to investigate 65nm technology capabilities
- **first test-prototypes** will be put on silicon in ~Spring 2014

Backup slides

Luminosity and Pile-Up (PU)

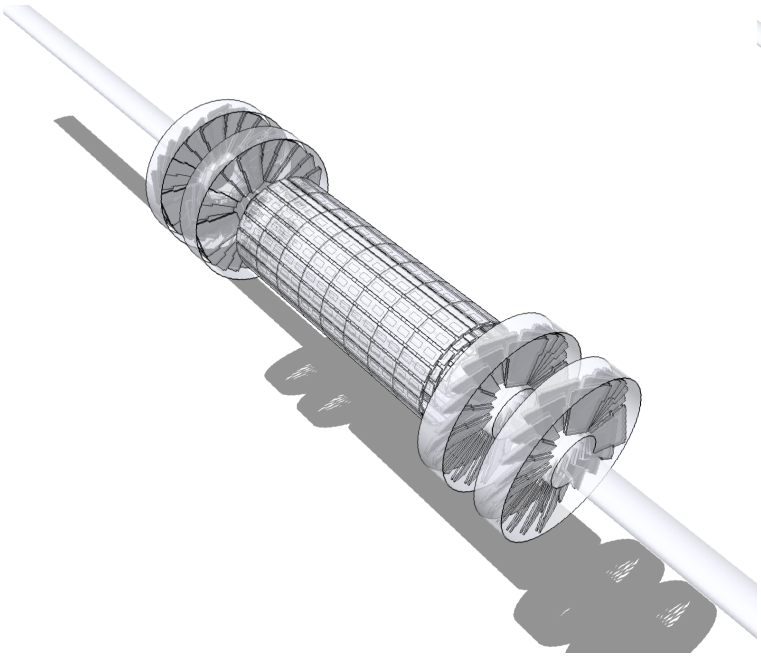


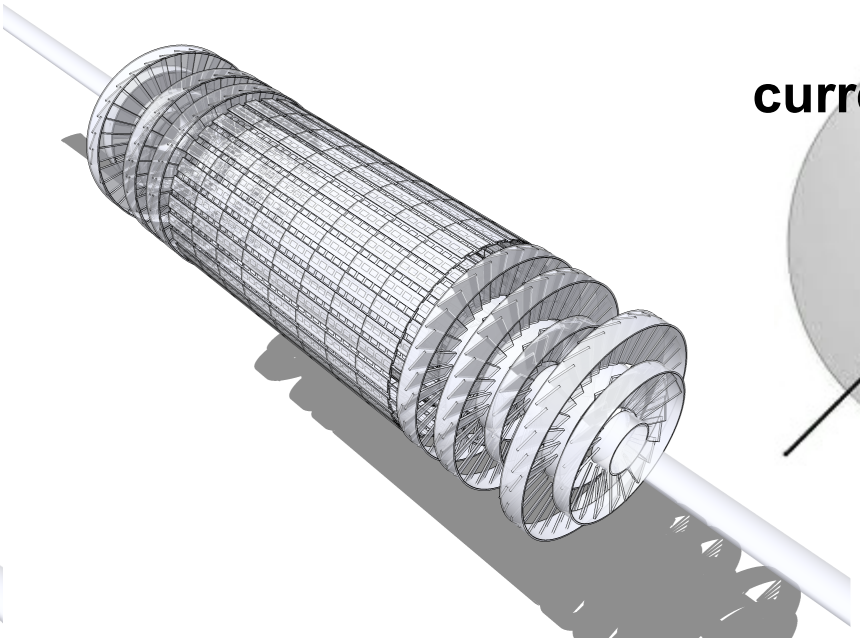


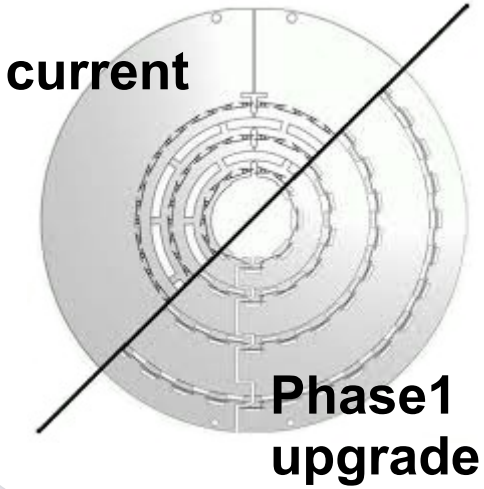
#interactions per BX = (total cross section x instantaneous luminosity) / bunch collision rate

Ex. **100 mb x 10^{35} cm^{-2} s^{-1} x 25 ns = 250 ! [1b = 10 fm x 10 fm = 10^{-24} cm^2]**

CMS Phase1 pixel upgrade



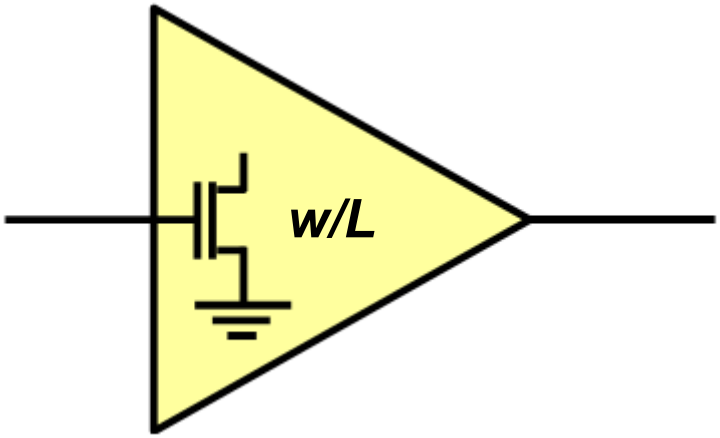




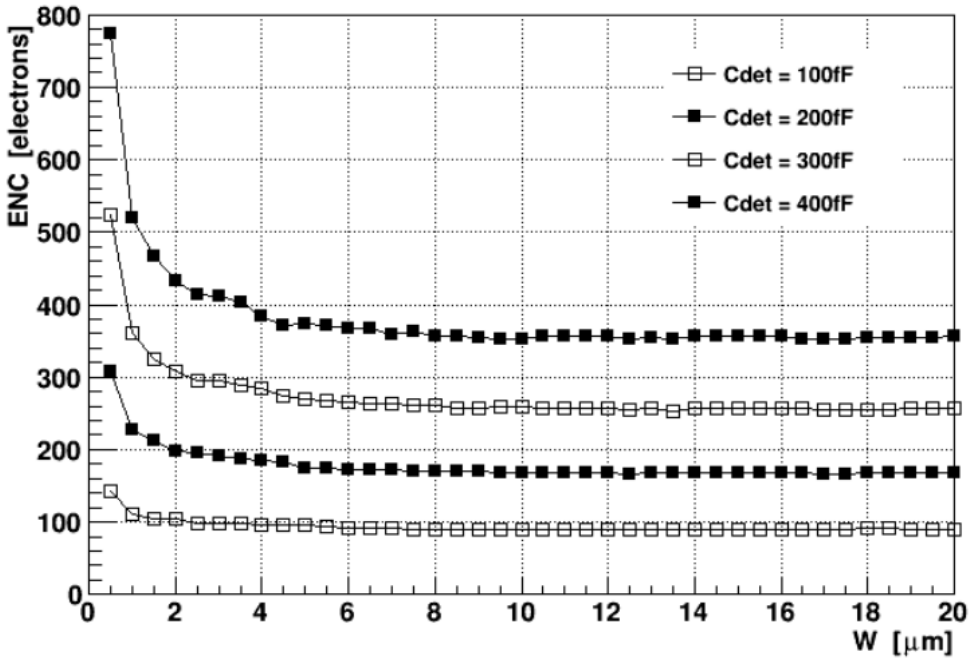
CMS **Phase1** pixel detector upgrade (end of 2016)

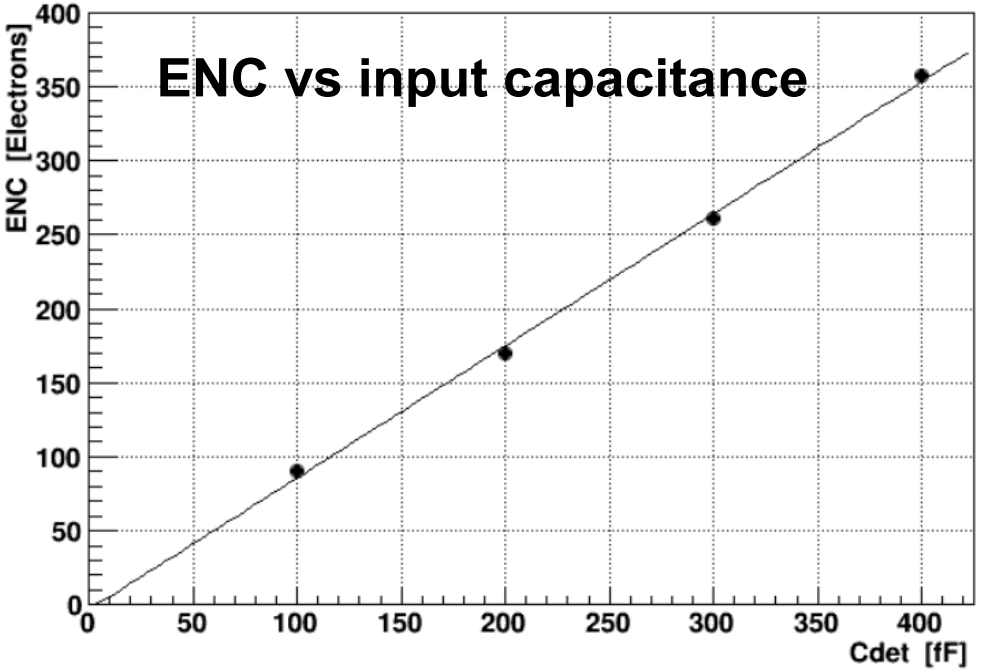
- BPIX: 3 → 4 layers
- FPIX: 2 → 4 disks
- pixel ASIC: improved version of the current PSI46v2 chip (PSI46v2DIG) to reduce data loss due to electronics readout

Input device noise optimization



- CSA core amplifier for classical **input device noise optimization**
- ENC ~100e RMS for 100 fF sensor capacitance





International schools

- Data Driven Front-End Electronics for Time and Energy Measurements with Highly Segmented Detectors
  Torino, Italy, Nov 25-27, 2013

- Low Power Analog IC Design Course
  EPFL, Lausanne, Switzerland, Jul 1-5, 2013

- CMS Data Analysis School (DAS)
  Pisa, Italy, Jan 23-27, 2012

Conferences and Workshops

- *International Workshop on Real Time, Self Triggered Front-End Electronics for Multichannel Detectors*
  Torino, Italy, Nov 27-28, 2013
- *Workshop su Elettronica VLSI nell' INFN*
  Padova, Italy, Nov 13, 2013
- *XCIX Congresso Nazionale Societa Italiana di Fisica (SIF)*
  Trieste, Italy, Sep 17, 2013
- *CMS Tracker Week*
  CERN, Switzerland, Feb 4-8, 2013
- *ATLAS/CMS 65nm pixel ASIC meeting*
  CERN, Switzerland, Nov 26-27, 2012
- *CMS Tracker Italian Workshop*
  Perugia, Italy, Mar 26-27, 2012

Publications

- Authorship within the CMS Collaboration since October 2013
  http://inspirehep.net

- *RD Collaboration Proposal: Development of Pixel Readout Integrated Circuits for Extreme Rate and Radiation*
  http://cds.cern.ch/record/1553467

- *CMS Technical Design Report for the Pixel Detector Upgrade*
  http://cds.cern.ch/record/1481838

Teaching assistance

A.A. 2013/2014

- LTspice tutorials (6 hours), Esperimentazioni II, M. Chiosso

A.A. 2012/2013

- PSpice tutorials (4 hours), Esperimentazioni II, M. Chiosso
- PSpice tutorials (5 hours), Elettronica, E. Menichetti
- lab. assistance (30 hours), LFNS II, M. Costa

A.A. 2011/2012

- PSpice tutorials (6 hours), Microelettronica, A. Rivetti