Development of Integrated Pixel Front-End Electronics in 65nm CMOS Technology for Extreme Rate and Radiation

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XVII cycle

2nd year seminar

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Turin, February 12, 2014
Outline

- Background, framework and motivations
- PhD research activity summary and status report
- Future work and outlook
Part I – Background, framework and motivations
The CMS experiment at LHC

Key:
- Blue: Muon
- Red: Electron
- Green: Charged Hadron (e.g., Pion)
- Olive: Neutral Hadron (e.g., Neutron)
- Dotted: Photon

Diagram showing different components of the CMS experiment, including the silicon tracker, electromagnetic calorimeter, hadron calorimeter, and superconducting solenoid.
Current CMS silicon pixel detector layout:

- 3 barrel layers (BPIX) + 2 forward disks each side (FPIX)
- coverage $|\eta| < 2.5$, ~ 1 m$^2$, 66 Mpixels
- track seeding, IP resolution, SV reconstruction
- **hybrid pixel detectors**
CMS hybrid pixel detectors

- $n^+$- on-n planar silicon sensors
- 100$\mu$m x 150$\mu$m pixel size
- 280$\mu$m thickness
- 300V nominal reverse bias
- charge collection by drift (speed and radiation hardness)
- the charge signal of each pixel is read out by its own dedicated Front-End Electronics (FEE)
- bump-bonding technique (flip-chip technology)

The readout of a pixel matrix requires the design of a high specialized full-custom Application-Specific Integrated Circuit (ASIC) implemented in Very Large Scale Integration (VLSI) CMOS technologies
CMOS fabrication processes dominate the market of Integrated Circuits (ICs).

The integration density doubles roughly every 2 years (Moore's Law).

CMOS technologies represent the standard solution for implementing radiation-hard Front-End electronics for particle physics applications in harsh radiation-sensitive environments.
CMS pixel Read-Out Chip (ROC)

0.25 μm 5M CMOS technology (PSI46v2)

Pixel Unit Cell (PUC)

- 52 x 80 pixels
- 9.8 mm x 7.9 mm
- 32 data buffers
- 12 timestamp buffers
- Double column periphery (data buffers, timestamp buffers)
- Control interface block & supply pads

Pixel array:
- 52 columns x 80 rows = 4160 pixels
- 26 double columns
3 main LHC commissioning periods referred to as **Phase0** (up to LS1), **Phase1** (after LS1) and **Phase2** (after LS3)

- **shutdown** time-slots for maintenance and machine performance improvements
  - nominal LHC: $10^{34}$ cm$^{-2}$ s$^{-1}$ luminosity, 23 fb$^{-1}$/year in 2012
  - **High-Luminosity (HL) LHC**: $10^{35}$ cm$^{-2}$ s$^{-1}$ luminosity, 300 fb$^{-1}$/year, foreseen 3000 fb$^{-1}$ in 10 years
The foreseen HL-LHC upgrade will introduce unprecedented operating conditions in terms of track densities (10x Phase0) and radiation levels (10x Phase0).
## CMS Phase 2 pixel upgrade motivations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>LHC Phase0</th>
<th>LHC Phase1</th>
<th>LHC Phase2</th>
</tr>
</thead>
<tbody>
<tr>
<td>luminosity</td>
<td>$10^{34}$ cm$^{-2}$ s$^{-1}$</td>
<td>$2 \times 10^{34}$ cm$^{-2}$ s$^{-1}$</td>
<td>$10^{35}$ cm$^{-2}$ s$^{-1}$</td>
</tr>
<tr>
<td>PU</td>
<td>~20</td>
<td>~50</td>
<td>140 or higher</td>
</tr>
<tr>
<td>particle flux</td>
<td>50 MHz/cm$^2$</td>
<td>200 MHz/cm$^2$</td>
<td>500 MHz/cm$^2$</td>
</tr>
<tr>
<td>pixel flux</td>
<td>200 MHz/cm$^2$</td>
<td>600 MHz/cm$^2$</td>
<td>1-2 GHz/cm$^2$</td>
</tr>
<tr>
<td>TID (10 years)</td>
<td>1.5 MGy</td>
<td>3.5 MGy</td>
<td>10 MGy</td>
</tr>
<tr>
<td>signal threshold</td>
<td>2.5-3 ke</td>
<td>1.5-2 ke</td>
<td>1 ke or below</td>
</tr>
<tr>
<td>L1 trigger latency</td>
<td>2-3 μs</td>
<td>4-6 μs</td>
<td>6-20 μs</td>
</tr>
</tbody>
</table>

The current PSI46v2 chip was designed about 10 years ago to work properly up to $2 \times 10^{34}$ cm$^{-2}$ s$^{-1}$ luminosity and for 100μm x 150μm pixels.

*design of a new pixel readout chip required for HL-LHC!*
Part II – PhD research work summary
Pixel Phase2 ROC

A

D

25 μm

100 μm

150 μm

2nd year seminar

PhD research topic
The design of such complex pixel ASICs is carried out with extensive usage of professional and industry-standard computer aided design (CAD) techniques for circuit simulation and IC mask design.
sensor choice not yet finalized:
- very likely planar sensors in the outer layers
- ongoing RD studies for innermost layers (thin planar sensors? 3D sensors? diamonds?)
- *sensor-independent* Front-End electronics

- certainly thinner planar silicon sensors to ensure adequate radiation tolerance
  - assume about 100μm thickness (1MIP ~10ke) for Phase2 (280μm current)
  - *low-noise* and *very low-threshold* Front-End electronics requirements

- 50 fF up to 300 fF total input capacitance
- 1'000e minimum detectable charge
New pixel ASIC requirements /2

- increased track densities
  - smaller pixel size for adequate granularity
  - assume 50μm x 100μm or 25μm x 100μm (100μm x 150μm current pixels)

- increased pixel rates (assume 2GHz/cm² particle flux)
  - 100kHz/pixel with 50μm x 100μm pixels or
  - 50kHz/pixel with 25μm x 100μm pixels

- larger amount of data
  - more on-pixel intelligence and local data storage capabilities
  - on-pixel trigger matching for zero suppression
  - possible contributions to the L1 trigger?

- 100kHz/pixel hit rate
- 25μm x 50μm analog area
- ~6μW/channel analog power budget
a commercial **65nm CMOS** has been chosen by the HEP **pixel community** as the present favored fabrication technology for the Phase2 generation of pixel ASICs

- present LHC experiments based on a commercial **CMOS 250nm**
- Phase1 LHC experiment upgrades will also exploit **CMOS 130nm** (e.g. FE-I4 chip for the ATLAS IBL, GBT project)
the **radiation tolerance** increases with technology scaling (thinner gate oxides)

radiation-hardened design techniques with Enclosed Layout Transistors (ELT) no more required

65nm demonstrated to be radiation tolerant up to 2 MGy TID, better than 130nm (now to be confirmed up to 10 MGy)
Why 65nm?

- **low power**
  - 1.2 V supply voltage as 130nm (2.5 V in 0.25μm)

- **a 65nm offers higher integration densities** w.r.t. 130nm
  - chance of implementing more **on-pixel intelligence** for efficient zero suppression schemes (on-pixel trigger matching)

- **improved speed** (~GHz)

- **mature technology**
  - introduced ~10 years ago
  - long term support and availability (OK for Phase2 ~2022)

- at present the 65nm represents **the most advanced technology node** adopted to implement full-custom solutions for radiation detection and measurements in particle physics and medical applications
similar requirements (and uncertainties) between ATLAS/CMS experiments Phase2 pixel upgrades

- joint ATLAS/CMS collaboration for sharing efforts in technology qualification
- collaboration extended to other groups interested in designing in 65nm

new **RD collaboration proposal** for the development of pixel ASICs in 65nm technology presented to the LHCC in June 2013

project now approved and officially supported by CERN as **RD53**

~ 20 institutes from around the world
  - about 100 collaborators, 50% ASIC designers
  - **strong Italian component** from INFN institutes (Bari, Bergamo/Pavia, Padova, Perugia, Pisa and Torino)
Italian CMS/ATLAS groups submitted in July 2013 a detailed proposal to INFN CSN5 to finance a new RD on CMOS 65nm for the next three years
- Bari, Milano, Padova, Bergamo/Pavia, Perugia, Pisa and Torino INFN institutes involved

CHIPIX65 approved in October 2013
- 700 kEuro funding, ~2 MPW submissions/year
- 35 members, 20 ASIC designers

Research activities divided into different working packages
- radiation hardness
- analog electronics
- digital electronics
- chip integration

First submission to the foundry planned for June/July 2014
2012/2013 research activity summary

**UNIX system administration** and support for CMS 65nm design activities in Turin
- design kit installation and maintenance
- CAD tools setup and usage

**65nm design kit test and characterization**
- full design-flow test and understanding
- technology and models characterization
- documentation

**design and simulation** of different analog and mixed-signal blocks
- high open-loop gain inverting amplifier for charge sensitive amplifier (CSA)
- track-and-latch comparator with autozeroing
- basic library of custom digital gates
- auxiliary digital control logic
- 5-bit SAR ADC with asynchronous control logic

65nm completely new in Turin!
digital design gains from **technology scaling** in terms of speed, integration density (higher functionality) and power/gate

**analog design more challenging**
- increased device-modeling complexity and number of **design rules**
- **short channel effects** cannot be neglected
- reduced **voltage headrooms** and single-transistor **intrinsic gain**
Pixel Front-End basics /Signal formation

- **charge-to-voltage conversion** provided by a charge-sensitive amplifier (CSA)
- further **signal shaping** and **noise reduction** can be achieved by means of a dedicated filtering stage (SHAPER)
- a complex **feedback network** is required to discharge the feedback capacitance and to compensate the sensor **leakage current**
Pixel Front-End basics /Analog pulse

gain = pulse amplitude / input charge

SNR = pulse amplitude / RMS noise

ENC = RMS noise / gain

baseline

peaking time

undershoot

RMS noise
Pixel Front-End basics /Hit discrimination

- yes / no? (binary readout)
- when? (time stamp)
- input charge?
1MIP ~10'000e for 100 μm thickness silicon sensors

Linearity OK up to 3MIPs
• try to explore **innovative solutions** for hit discrimination and charge encoding
• take advantage of the **speed** offered by a **65nm CMOS**
• what about a **synchronous** Front-End approach?
Minimum detectable charge signal

- the challenge is to discriminate pulses of a few mV above the nominal threshold
- requires the design of a **high-speed (~1ns)** and **high-resolution (~mV)** comparator

1'000e charge signal
100 fF input capacitance

nominal threshold = 5 x RMS noise

~10 mV

~1 mV RMS noise

~30ns
Positive feedback

\[ V_{x,y} (t=0) \]

- \( V_x (0) > V_y (0) \)
- \( V_x (0) < V_y (0) \)
thanks to the usage of positive feedback the comparator decision is promptly ready within ~ 1ns
fast signals of a few mV above the nominal threshold can be discriminated
Synchronous Front-End approach

Continuous-time comparator

Track-and-latch comparator
hit generation synchronized with a 25ns bunch crossing (12.5ns peaking time)

the delay becomes an almost constant and well defined quantity ~peaking time

no time-walk issues in the time stamp assignment
Complete analog chain simulation
Layout example

LATCH

4 μm

8 μm

Vout1  Vout2

Vin1  Vin2
Conclusions and outlook
Next steps and future work

- the CHIPIX65 collaboration is planning to submit a 3mm x 4mm Multi Project Wafer (MPW) to the foundry in ~Spring 2014

- design of an innovative charge encoding based on a local asynchronous digital control logic for ToT measurements

- on-line calibration with autozeroing techniques is under investigation

- finalization of the complete layout for the analog part

- test-bench characterization and measurements with first prototypes
my PhD research activity is devoted to the design of innovative solutions for pixel ASIC analog Front-End electronics suitable for the foreseen Phase2 CMS pixel upgrade.

a commercial 65nm CMOS has been chosen by the HEP pixel community as the present favored fabrication technology for the next generation of pixel ASICs.

at present the 65nm represents the most advanced technology node adopted to implement full-custom solutions for radiation detection and measurements in particle physics and medical applications.

new 3-years joint ATLAS/CMS collaborations RD53 and CHIPIX65 are devoted to investigate 65nm technology capabilities.

first test-prototypes will be put on silicon in ~Spring 2014.
Backup slides
Luminosity and Pile-Up (PU)

\[ \sigma \sim 85 \text{ mb} @ \sqrt{s} = 7 \text{ TeV} \]
\[ \sigma \sim 100 \text{ mb} @ \sqrt{s} = 14 \text{ TeV} \]

#interactions per BX = (total cross section x instantaneous luminosity) / bunch collision rate

**Ex.** \( 100 \text{ mb} \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1} \times 25 \text{ ns} = 250 ! \quad [1b = 10 \text{ fm} \times 10 \text{ fm} = 10^{-24} \text{ cm}^2] \)
CMS Phase1 pixel detector upgrade (end of 2016)

- BPIX: 3 → 4 layers
- FPIX: 2 → 4 disks
- pixel ASIC: improved version of the current PSI46v2 chip (PSI46v2DIG) to reduce data loss due to electronics readout
Input device noise optimization

- CSA core amplifier for classical input device noise optimization
- ENC ~100e RMS for 100 fF sensor capacitance

Graphs showing ENC vs input capacitance and W [μm].
International schools

- **Data Driven Front-End Electronics for Time and Energy Measurements with Highly Segmented Detectors**
  Torino, Italy, Nov 25-27, 2013

- **Low Power Analog IC Design Course**
  EPFL, Lausanne, Switzerland, Jul 1-5, 2013

- **CMS Data Analysis School (DAS)**
  Pisa, Italy, Jan 23-27, 2012
Conferences and Workshops

- **International Workshop on Real Time, Self Triggered Front-End Electronics for Multichannel Detectors**
  Torino, Italy, Nov 27-28, 2013

- **Workshop su Elettronica VLSI nell' INFN**
  Padova, Italy, Nov 13, 2013

- **XCIX Congresso Nazionale Societa Italiana di Fisica (SIF)**
  Trieste, Italy, Sep 17, 2013

- **CMS Tracker Week**
  CERN, Switzerland, Feb 4-8, 2013

- **ATLAS/CMS 65nm pixel ASIC meeting**
  CERN, Switzerland, Nov 26-27, 2012

- **CMS Tracker Italian Workshop**
  Perugia, Italy, Mar 26-27, 2012
Authorship within the CMS Collaboration since October 2013
http://inspirehep.net

RD Collaboration Proposal: Development of Pixel Readout Integrated Circuits for Extreme Rate and Radiation
http://cds.cern.ch/record/1553467

CMS Technical Design Report for the Pixel Detector Upgrade
http://cds.cern.ch/record/1481838
Teaching assistance

A.A. 2013/2014
- LTspice tutorials (6 hours), Esperimentazioni II, M. Chiosso

A.A. 2012/2013
- PSpice tutorials (4 hours), Esperimentazioni II, M. Chiosso
- PSpice tutorials (5 hours), Elettronica, E. Menichetti
- lab. assistance (30 hours), LFNS II, M. Costa

A.A. 2011/2012
- PSpice tutorials (6 hours), Microelettronica, A. Rivetti